CompactFlash™ Card

Product Specification

V4.2

Contents:

1. Scope

This document describes the features and specifications and installation guide of CompactFlash™ Card products. In the appendix, there provides order information, warranty policy, RMA/DOA procedure for the most convenient reference.

2. Introduction

CompactFlash™ Cards are design base on CompactFlash™ Card Specification 3.0 compliant. It make up of a flash memory controller and NAND-Type flash memory. It can support a capacity of 128MB, 256MB, 512MB, 1GB, 2GB, 4GB, 8GB, 16GB, 32GB. The CompactFlash card come with commercial operating temperature grad (0℃~+70 ℃) and industrial operating temperature grad (-40℃~+85℃) to fulfill various specialized applications in normal or harsh operating environments. CompactFlash™ Card is ideal solutions for critical applications which request for long term supply with consistent key components.

3. System Features

- CompactFlash™ Card Specification 3.0 compliant
- Operating Modes:
  - PC Card Memory Mode.
  - PC Card I/O Mode.
  - True-IDE Mode.
- Ultra DMA Mode supported up to Mode 4.
- High reliability assured based on the internal Error Correcting Code (ECC) function.
- Auto Standby and Sleep Mode supported.
- Reliable wear-leveling algorithm to ensure the best of flash endurance.
- Very low power consumption
- Very high performance
- Rugged environment is working well
- Automatic error correction and retry capabilities
- Supports power down commands and Auto Stand-by / Sleep Mode
- +5 V ±10％ or +3.3 V ±5％ operation
- Low weight
- Noiseless
- MTBF > 2,000,000 hours
- Minimum 10,000 insertions
- Support O/S: Windows 31/95/98/Me, Windows NT/2000/XP/2003, WinCE, QNX, Linux, DOS and more
- Capacity:
  128MB, 256MB, 512 MB, 1GB, 2GB, 4GB, 8GB, 16GB, and 32GB(unformatted)

4. Product Specifications

For all the following specifications, values are defined at ambient temperature and nominal supply voltage unless otherwise stated.

4.1. System Environmental Specification

		Standard Temperature	Wide Temperature
Referral Part Number		CFC-50SUXXXX[1]BPCY[2]	CFC-50SUXXXX[1]BPIY[2]
Temperature	Operating: Non-operating:	0ºC ~ +70ºC -20ºC ~ +85ºC	-40ºC ~ +85ºC -50ºC ~ +95ºC
Humidity	Operating & Non-operating:	5% ~ 95% non-condensing	
Vibration	Operating & Non-operating:	20G peak-to-peak maximum	
Shock	Operating & Non-operating:	1500 G maximum	
Altitude	Operating & Non-operating:	50,000 feet maximum	

Note:
XXXX:128M, 256M, 512M, 001G, 002G, 004G, 008G, 016G, 032G
Y:F(Fixed Disk Mode), R(Removable Disk Mode); A(Auto Detect Disk Mode)

4.2. System Power Requirement

		Standard Temperature		Wide Temperature	
Referral Part Number		CFC-50SUXXXX[1]BPCY[2]		CFC-50SUXXXX[1]BPIY[2]	
DC Input Voltage 100mV max. ripple (p-p)		3.3V±5%	5V±10%	3.3V±5%	5V±10%
+5V Current (Maximum average value)	Sleeping Mode:	2.3mA(Typ.)	2.3mA(Typ.)	2.3mA(Typ.)	2.3mA(Typ.)
	Reading Mode:	57.7mA(Typ)	57.7mA(Typ)	57.7mA(Typ)	57.7mA(Typ)
	Writing Mode:	60mA(Typ)	60mA(Typ)	60mA(Typ)	60mA(Typ)
XXXX:128M, 256M, 512M, 001G, 002G, 004G, 008G					

Note:
XXXX:128M, 256M, 512M, 001G, 002G, 004G, 008G, 016G, 032G
Y:F(Fixed Disk Mode), R(Removable Disk Mode); A(Auto Detect Disk Mode)

4.3. System Performance

Data Transfer Rate To/From Flash		20Mbytes /sec burst
Data Transfer Rate To/From Host	Ultra DMA mode 4	66.6 Mbytes /sec burst
	PIO mode 4	16.6Mbytes /sec burst
Maximum Performance	Sequential Read	29Mbytes / sec Max.
	Sequential Write	19Mbytes / sec Max.

Note:
(1). All values quoted are typical at 25ºC and nominal supply voltage.
(2). Sleeping mode currently is specified under the condition that all card inputs are static CMOS levels and in a "Not Busy" operating state.

4.4. System Reliability

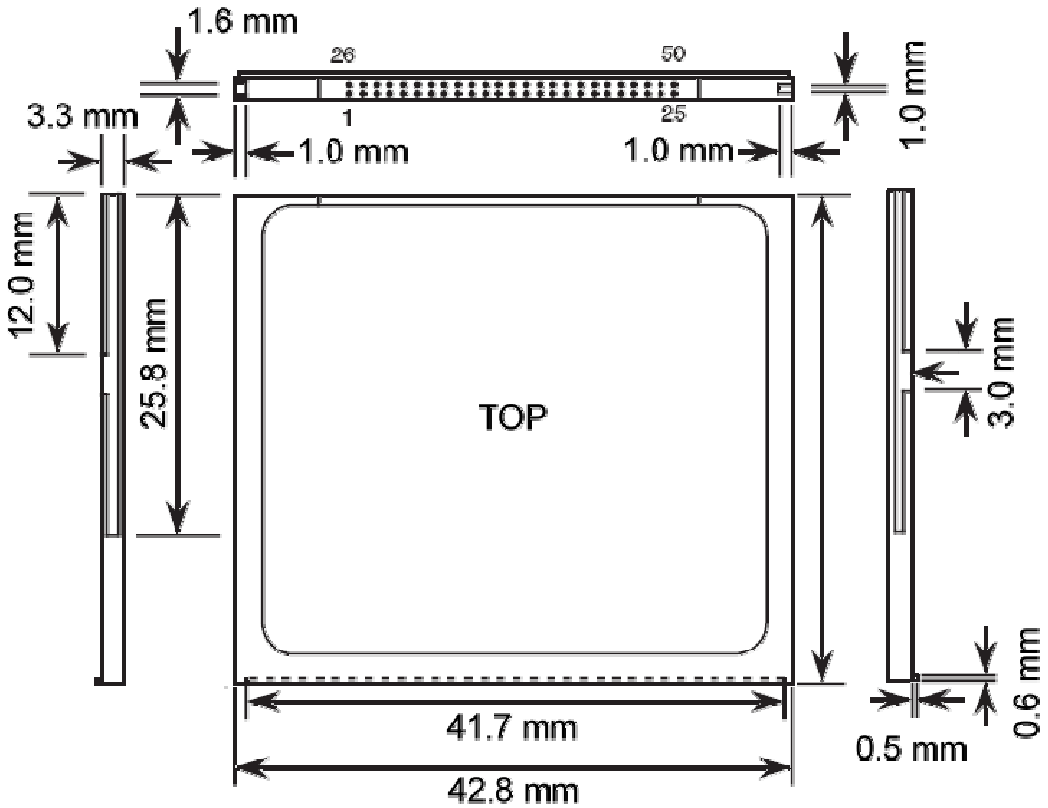
MTBF	**> 2,000,000 hours**
Data Reliability	**< 1 non-recoverable error in 10^{14} bits read** **< 1 erroneous correction in 10^{20} bits read**
Wear-leveling Algorithms	**Supportive**
ECC Technology	**4 bits Error Connection Code**
Endurance	**Greater than 2,000,000 cycles Logically contributed by Wear-leveling and advanced bad sector management**
Data Retention	**10 years**

4.5. Physical Specifications

4.5.1. Physical Specifications

CompactFlash™ Card	
Length:	36.40 ± 0.15 mm (1.433 ±.006 in)
Width:	42.80 ± 0.10 mm (1.685 ±.004 in)
Thickness:	3.3 mm ± 0.10 mm (.130 ±.004 in) (Excluding Lip)
Weight:	11.4 g (.40 oz) typical, 14.2 g (.50 oz) maximum

4.5.2. Dimension



4.6. Capacity Specification

4.6.1. The specific capacity for the various models and the default number of heads, sectors/track and cylinders.

Unformatted Capacity	Default Cylinder	Default Head	Default Sector	Defaulted CHS Capacity
128MB	978	8	32	128,188,416
256MB	978	16	32	256,376,832
512MB	993	16	63	512,483,328
1GB	1,985	16	63	1,024,450,560
2GB	3,954	16	63	2,040,643,584
4GB	7,889	16	63	4,071,481,344
8GB	15,778	16	63	8,142,962,688

5. Interface Description

5.1. Pin Assignments

	Memory card mode		I/O card mode		True IDE mode	
Pin NO.	**Signal name**	**I/O**	**Signal name**	**I/O**	**Signal name**	**I/O**
1	GND	—	GND	—	GND	—
2	D3	I/O	D3	I/O	D3	I/O
3	D4	I/O	D4	I/O	D4	I/O
4	D5	I/O	D5	I/O	D5	I/O
5	D6	I/O	D6	I/O	D6	I/O
6	D7	I/O	D7	I/O	D7	I/O
7	-CE1	I	-CE1	I	-CE0	I
8	A10	I	A10	I	A10[2]	I
9	-OE	I	-OE	I	-ATA SEL	I
10	A9	I	A9	I	A9[2]	I
11	A8	I	A8	I	A8[2]	I
12	A7	I	A7	I	A7[2]	I
13	VCC	—	VCC	—	VCC	—

14	A6	I	A6	I	A6[2]	I
15	A5	I	A5	I	A5[2]	I
16	A4	I	A4	I	A4[2]	I
17	A3	I	A3	I	A3[2]	I
18	A2	I	A2	I	A2	I
19	A1	I	A1	I	A1	I
20	A0	I	A0	I	A0	I
21	D0	I/O	D0	I/O	D0	I/O
22	D1	I/O	D1	I/O	D1	I/O
23	D2	I/O	D2	I/O	D2	I/O
24	WP	O	-IOIS16	O	-IOCS16	O
25	-CD2	O	-CD2	O	-CD2	O
26	-CD1	O	-CD1	O	-CD1	O
27	D11[1]	I/O	D11[1]	I/O	D11[1]	I/O
28	D12[1]	I/O	D12[1]	I/O	D12[1]	I/O
29	D13[1]	I/O	D13[1]	I/O	D13[1]	I/O
	Memory card mode		**I/O card mode**		**True IDE mode**	
Pin NO.	**Signal name**	**I/O**	**Signal name**	**I/O**	**Signal name**	**I/O**
30	D14[1]	I/O	D14[1]	I/O	D14[1]	I/O
31	D15[1]	I/O	D15[1]	I/O	D15[1]	I/O
32	-CE2[1]	I	-CE2[1]	I	-CE1[1]	I
33	-VS1	O	-VS1	O	-VS1	O
34	-IORD	I	-IORD	I	-IORD[7] HSTROBE[8] -HDMARDY[9]	I
35	-IOWR	I	-IOWR	I	-IOWR[7] STOP[8, 9]	I
36	-WE	I	-WE	I	-WE[3]	I
37	RDY/-BSY	O	-IREQ	O	INTRQ	O
38	VCC	—	VCC	—	VCC	—
39	-CSEL[5]	I	-CSEL[5]	I	-CSEL	I
40	-VS2	O	-VS2	O	-VS2	O
41	RESET	I	RESET	I	-RESET	I
42	-WAIT	O	-WAIT	O	-IORDY[7] -DDMARDY[8]	O

					DSTROBE[9]	
43	-INPACK	O	-INPACK	O	DMARQ	O
44	-REG	I	-REG	I	-DMACK[6]	I
45	BVD2	I/O	-SPKR	I/O	-DASP	I/O
46	BVD1	I/O	-STSCHG	I/O	-PDIAG	I/O
47	D8[1]	I/O	D8[1]	I/O	D8[1]	I/O
48	D9[1]	I/O	D9[1]	I/O	D9[1]	I/O
49	D10[1]	I/O	D10[1]	I/O	D10[1]	I/O
50	GND	—	GND	—	GND	—

Note:

1) *These signals are required only for 16 bit accesses and not required when installed in 8 bit systems. Devices should allow for 3-state signals not to consume current.*
2) *The signal should be grounded by the host.*
3) *The signal should be tied to VCC by the host.*
4) *The mode is optional for CF+ Cards, but required for CompactFlash™ Storage Cards.*
5) *The -CSEL signal is ignored by the card in PC Card modes. However, because it is not pulled up on the card in these modes, it should not be left floating by the host in PC Card modes. In these modes, the pin should be connected by the host to PC Card A25 or grounded by the host.*
6) *If DMA operations are not used, the signal should be held high or tied to VCC by the host. For proper operation in older hosts: while DMA operations are not active, the card shall ignore this signal, including a floating condition*
7) *Signal usage in True IDE Mode except when Ultra DMA mode protocol is active.*
8) *Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Write is active.*
9) *Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Read is active.*

5.2. Pin Descriptions

Signal Name	Dir	Pin No.	Description
A10 to A0 (PC Card Memory Mode)	I	8,10,11,12,14,15,16 ,17,18,19,20	These address lines along with the-REG signal are used to select the following: The I/O port address registers within the CompactFlash™ Storage Card or CF + Card, the memory mapped port add address registers within the CompactFlash™ Storage Card or CF+ Card , a byte in the card's information structure and its configuration control and status registers.
A10 to A0 (PC Card I/O Mode)			
A2 to A0 (True IDE Mode)		18,19,20	In True IDE Mode only {2:0} are used to select the one of eight registers in the Task File. The remaining address lines should be grounded by the host.
BVD1 (PC Card Memory mode)	I/O	46	This signal is asserted high as BVD1 is not supported.

-STSCHG (PC Card Memory Mode)			This Signal is asserted low to alert the host to changes in the RDY/-BSY and Write Protect states; while the I/O interface is configured. Its use is controlled by the Card Configured and Status Register.
-PDIAG (True IDE Mode)			In the True IDE Mode, this input/output is the Pass Diagnostic signal in the Master/Slave handshake protocol.
Signal Name	**Dir**	**Pin No.**	**Description**
BVD2 (PC Card Memory Mode)	I/O	45	This signal is asserted high, as BVD2 is not supported.
-SPKR (PC Card I/O Mode)			This line is Binary AUDIO OUTPUT From the Card. If the Card doesn't support the Binary Audio function, this line should be held negated.
-DASP (True IDE Mode)			In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave.
-CD1, -CD2 (PC Card Memory Mode)	O	25,26	These Card Detect pins are connected to ground on the CompactFlash™ Storage Card or CF+ Card. They are used by the host to determined that the CompactFlash™ Storage Card or CF+ Card is fully inserted into its socket.
-CE1,-CE2 (PC Card Memory Mode)	I	7,32	There input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. –CE2 always accesses the odd byte of the word depending on A0 and –CE2. A multiplexing scheme based on A1. –DE1, -CE2 allow 8-bit hosts to access all data on D0 to D7. See Access Specification below.
-CE1,-CE2 (PC Card I/O Mode)			
-CS0,-CS1 (True IDE Mode)			In the True IDE Mode CS0 is the chip select for the task file registers while CS1 is used to select the Alternate Status Register and Device Control Register.
-CSEL (PC Card Memory Mode)	I	39	This signal is not used for this mode.
-CSEL (PC Card I/O Mode)			This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.
-CSEL (True IDE Mode)			
D15 to D00 (PC Card Memory Mode)	I/O	31,30,29,38,37,49,48,48,6,5,4,3,2,23,22,21	These lines carry the Data, commands and Status information between the host and the controller. D00 is the LSB of the Even Byte of the Word
D15 to D00			

(PC Card I/O Mode)			D08 is the LSB of the Odd Byte of the Word.
D15 to D00 (True IDE Mode)			True IDE Mode, all Task File operations occur in byte mode on the low order bus D00 to D07 while all data transfers are 16 but using D00 to D15.
Signal Name	**Dir**	**Pin No.**	**Description**
GND (PC Card Memory Mode)	-	1,50	Ground
GND (PC Card I/O Mode)			
GND (True IDE Mode)			
-INPCAK (PC Card Memory Mode)	O	43	This signal is not used in this Mode.
-INPACK (PC Card I/O Mode)			The Input Acknowledge signal is asserted by the CompactFlash™ Storage Card or CF+ Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the CompactFlash™ Storage Card or CF+ Card and the CPU.
-INPACK (True IDE Mode)			In True IDE Mode this output signal is not used and should not be connected at the host.
-IORD (PC Card Memory Mode)	I	34	This signal is not used in this mode.
-IORD (PC Card I/O Mode)			This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the CompactFlash™ Storage Card or CF+ Card when the card is configured to use the I/O interface.
-IORD (True IDE Mode)			In True IDE Mode, this signal has same function as in PC Card I/O Mode.
-IOWR (PC Card Memory Mode)	I	35	This signal is not used in this mode.
-IOWR (PC Card I/O Mode)			The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the CompactFlash™ Storage Card or CF+ Card controller registers when he Compact Storage Card or CF+ Card is configured to use the I/O interface. The clocking will occur on the negative to positive edge of the signal (Trailing edge).

Signal Name	Dir	Pin No.	Description
-IOWR (True IDE Mode)			In True IDE Mode, this signal has the same function as in PC Card I/O Mode.
Signal Name	**Dir**	**Pin No.**	**Description**
-OE (PC Card Memory Mode)	I	9	This is an Output Enable strobe generated by the host interface. It is used to read data from the CompactFlash™ Storage Card or CF+ Card in Memory Mode and to read the CIS and configuration registers.
-OE (PC Card I/O Mode)			In PC Card I/O Mode. This signal is used to read the CIS and configuration registers.
-ATA SEL (True IDE Mode)			To enable True IDE Mode this input should be grounded by the host.
PDY/BSY (PC Card Memory Mode)	O	37	In Memory Mode this signal is set high when the CompactFlash™ Storage Card or CF+ Card is ready to accept a new data transfer operation and held low when the card is busy. Theo Host memory card socket must provide a pull-up resistor. At power up and at Reset the RDY/-BSY signal is held low (busy) until the CompactFlash™ Storage Card or CF+ Card has completed its power up or reset function. No access of any type should be made to the CompactFlash™ Storage Card or CF+ Card during this time. The RDY/-BSY signal is held high (disabled from being busy) whenever the following condition is true. The CompactFlash™ Storage Card or CF+ Card has been powered up with + RESET continuously disconnected or asserted.
-IREQ (PC Card I/O Mode)			Operation – After the CompactFlash™ Storage Card or CF+ Card has been configured for I/O operational this signal is used as interrupt Request. This line is strobe low to generate a pulse mode interrupt or held low for a level mode interrupt.
INTRO (True IDE Mode)			In True IDE Mode signal is the active high interrupt Request to the host.

-REG (PC Card Memory Mode)	I	44	This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory. Low for Attribute Memory.
-REG (PC Card I/O Mode)			The signal must also be active (low) during I/O Cycles when the I/O address is on the Bus.
-REG (True IDE Mode)			In the True IDE Mode this input pin is the active low hardware reset from the host.

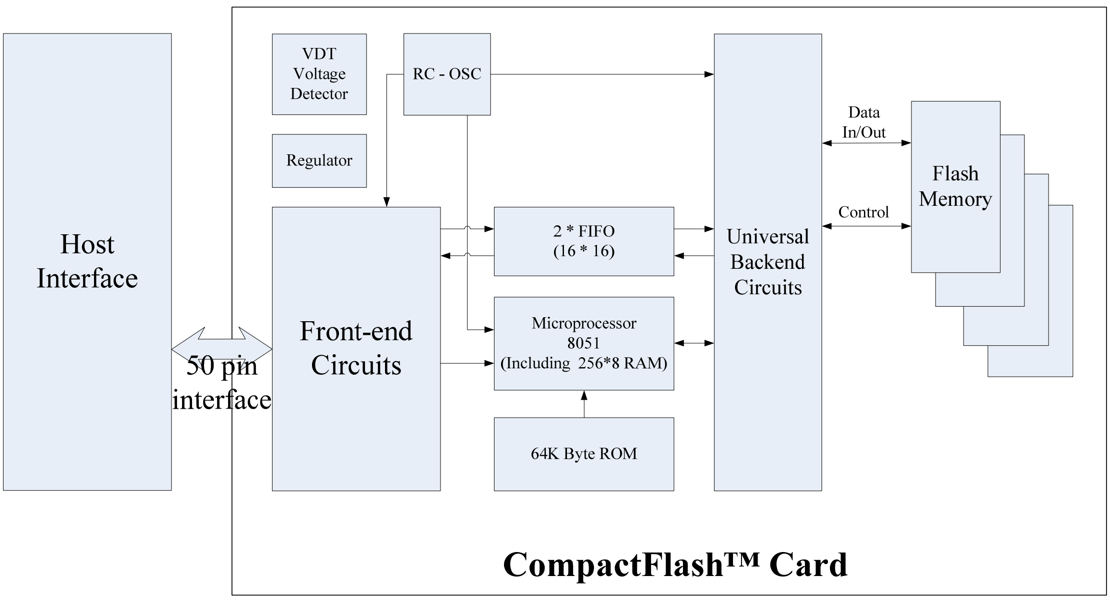
Signal Name	**Dir**	**Pin No.**	**Description**
RESET (PC Card Memory Mode)	I	41	When the pin is high, this signal Resets the CompactFlash™ Storage Card or CF+ Card. The CompactFlash™ Card or CF+ Car is Reset only at power up if this pin is left high or open from power-up. The CompactFlash™ Storage CF Card or CF+ Card is also Reset when the Soft Reset bit in the Card Configuration Option Register is set.
RESET (PC Card I/O Mode)			
RESET (True IDE Mode)			In the True IDE Mode this input pin is the active low hardware reset from the host.
VCC (PC Card Memory Mode) (PC Card I/O Mode) (True IDE Mode)	-	13,38	+5V, +3.3V power
-VS1/-VS2 (PC Card Memory Mode) (PC Card I/O Mode) (True IDE Mode)	O	3,40	Voltage Sense Signals. – VS1 is grounded o that the CompactFlash™ Storage Card or CF+ Card CIS can be read at 3.3 volts and –VS2 is reserved by PCMCIA for a secondary voltage.
-WAIT (PC Card Memory Mode)	O	42	The –Wait signal is driven low by the CompactFlash™ Storage Card or CF+ Card to signal the host to delay completion of a memory or I/O cycles that is in progress.
IORDY (True IDE Mode)			In True IDE Mode this output signal may be used as IORDY.
-WE (PC Card Memory Mode)	I	36	This is a signal driven by the host and used for starting memory write data to the registers of the CompactFlash™ Storage Card or CF+ Card when the card is configured I the memory interface mode. It is also used for writing the configuration registers.

-WE (PC Card I/O Mode)			In PC Card I/O Mode, this signal is used for writing the configuration registers.
-WE (True IDE Mode)			In True IDE Mode this input signal is not used and should be connected to VCC by the Host.
Signal Name	**Dir**	**Pin No.**	**Description**
WP (PC Card Memory Mode)	O	24	Memory Mode-The CompactFlash™ Storage Card or CF+ Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence.
-IOIS16 (PC Card I/O Mode)			I/O Operation-When the CompactFlash™ Storage Card or CF+ Card is configured for I/O operation Pin 24 is used for the – I/O Selected is 16 Bit Port (-IOIS1) function. A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port.
-IOIS16 (True IDE Mode)			In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.

5.3. CompactFlash™ I/O Mapping Address

PTnREG	Primary I/O PIHA[10:0]	Secondary I/O PIHA[10:0]	Independent I/O PIHA[3:0]	PInIORD = L	PInIOWR = L
L	1F0H	170H	0H	Read Even Data	Write Even Data
L	1F1H	171H	1H	Error Register	Feature Register
L	1F2H	172H	2H	Sector Count	Sector Count
L	1F3H	173H	3H	Sector Number	Sector Number
L	1F4H	174H	4H	Cylinder Low	Cylinder Low
L	1F5H	175H	5H	Cylinder High	Cylinder High
L	1F6H	176H	6H	Drive/Head	Drive/Head
L	1F7H	177H	7H	Status Register	Command
L	------	------	8H	Duplicate Read Even Data	Duplicate Write Even Data
L	------	------	9H	Duplicate Read Odd Data	Duplicate Write Odd Data
L	------	------	0DH	Duplicate Error	Duplicate Feature
L	3F6H	376H	0EH	Alternate Status	Device Control
L	3F7H	377H	0FH	Drive Address	Reserved

5.4. Card Block Diagram



6. Electrical Specification

The following table defines all D.C. Characteristics for the CompactFlash™ Series. The conditions are:

Commercial Temperature Products	Industrial Temperature Products
Vcc = 5V ±10% Vcc = 3.3V ± 5% Ta = 0°C to 70°C	Vcc = 5V ± 10% Vcc = 3.3V ± 5% Ta = -40°C to 85°C

6.1. Power Pin Description

Pin Name	I/O	Description
VCCQ	Power	Host VCC
VCC 3.3V	Power	3.3V VCC
GND	Power	GND

6.2. Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_{CC}	-0.3 to 5.5	V
Input Voltage	V_{IN}	-0.3 to V_{CC} +0.3	V
Output Voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V
Power Supply for Host I/O	Vccq	-0.6 to 6.0	V
Input Voltage for Host I/O	V_{IN_Host}	-0.3 to Vccq+0.3	V
Output Voltage for Host I/O	V_{OUT_Host}	-0.3 to Vccq+0.3	V
Soldering Temperature	T_{SOLDER}	260	℃
Storage Temperature	T_{STG}	-55 to 150	℃
Operating Temperature	T_{OPR}	0 to 70	℃

6.3. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Input Voltage	V_{IN}	-0.3	-	V_{CC} +0.3	V
Power Supply for Host I/O	Vccq	3.0	-	5.5	V
Input Voltage for Host I/O	V_{IN_Host}	-0.3	-	Vccq +0.3	V

6.4. DC Characteristics

(TOPRI= -40℃ to 85℃, Vcc=3.0V to 3.6V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Leakage Current	I_{IL}	No pull-up or pull-down	-1	-	1	μA
Tri-State Leakage Current	I_{OZ}		-1	-	1	μA
Input Capacitance*3	C_{IN}	V_{IN} =0V, f=1MHz			15	pF
Output Capacitance*3	C_{OUT}	V_{OUT} =0V, f=1MHz			15	pF
Input Low Voltage	V_{IL}	CMOS*1			0.2* V_{CC}	V
Input High Voltage	V_{IH}	CMOS*1	2.0			V
Host I/F Input Low Voltage	V_{ILQ}	TTL*2			0.8	V
Host I/F Input High Voltage	V_{IHQ}	TTL*2	2.0			V
Schmitt trigger negative going threshold voltage	Vt-	CMOS*1	0.9			V
		Vccq*2	0.8			V
Schmitt trigger positive going threshold voltage	Vt+	CMOS*1			2.5	V
		Vccq*2			2.0	V
Schmitt trigger negative going threshold voltage	Vt-	Vcc*1	0.9			V
Schmitt trigger positive going threshold voltage	Vt+	Vcc*1			2.5	V
Output Low Voltage	V_{OL}	I_{OL}=4.8mA			0.4	V
Output High Voltage	V_{OH}	I_{OH}=4.8mA	Vcc-0.8			V
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Host I/F Output Low	V_{OLQ}	I_{OL}=4.8mA			0.4	V

Voltage						
Host I/F Output high Voltage	V_{OHQ}	I_{OH}=4.8mA	Vcc-0.8			V
Input Pull-up/down resistance	Rt	V_{IL}=0V or V_{IH}=Vcc		75		KΩ
Active Current	I_{ACT}			75	95	mA
Sleep Current	I_{SLP}			0.5	3	mA
Power Regulator						
Regulator Output Voltage	V_{RO}	I_{load} =150mA	2.7	3.3	3.45	V
		I_{load} =150mA Vccq *2	3.15	3.3	3.45	V
Regulator Standby Current	I_{RSTB}				160	μA
Regulator Output Current	I_{RLOAD}				150	mA
RC Oscillator						
OSC frequency	f_{OSC}	Rext=39KΩ	83	85	87	MHz
Low Voltage Detector						
Rise Release Voltage	V_{RR}			2.89		V
Power Low Detect Voltage	V_{DET}		2.5	2.6	2.7	V

Note:

1. ***For the pins, which were driven by Vcc.***
2. ***For the host interface pins only, when Vccq = 4.5V to 5.5V***
3. ***This parameter is sampled and not 100% tested.***

6.5. AC Characteristics

(TOPRI= -40℃ to 85℃, Vcc=3.0V to 3.6V, Vccq=4.5V to 5.5V, output loading=35pF)

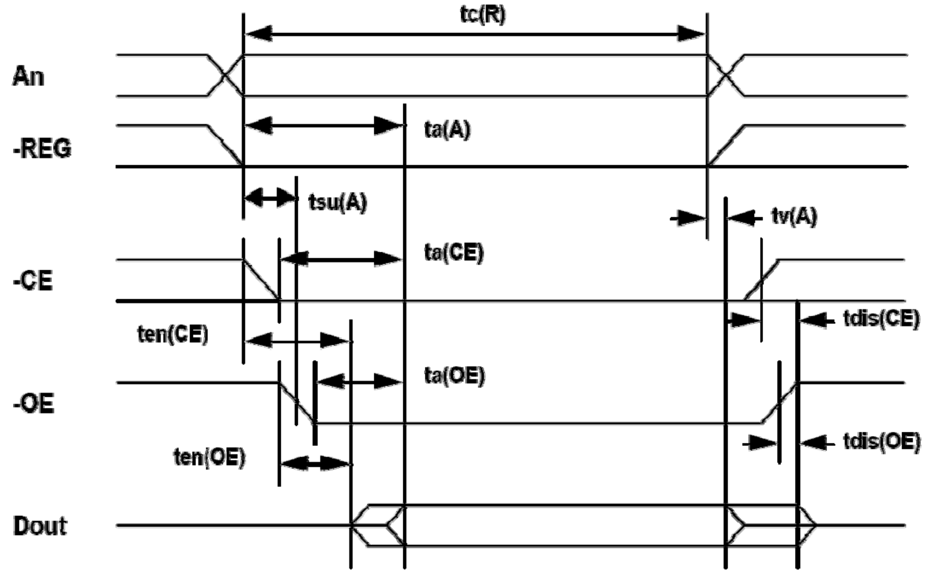
(1) Attribute Memory Read Timing Specification

Attribute Memory access time is defined as 300 ns.

Speed Version			300 ns	
Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Read Cycle Time	tc(R)	tAVAV	300	
Address Access Time	ta(A)	tAVQV		300
Card Enable Access Time	ta(CE)	tELQV		300
Output Enable Access Time	ta(OE)	tGLQV		150
Output Disable Time from CE	tdis(CE)	tEHQZ		100
Output Disable Time from OE	tdis(OE)	tGHQZ		100
Address Setup Time	tsu (A)	tAVGL	30	
Output Enable Time from CE	ten(CE)	tELQNZ	5	
Output Enable Time from OE	ten(OE)	tGLQNZ	5	
Data Valid from Address Change	tv(A)	tAXQX	0	

Note:

All times are in nanoseconds. Dout signifies data provided by the CompactFlash Storage Card or CF+ Card to the system. The -CE signal or both the -OE signal and the -WE signal shall be de-asserted between consecutive cycle operations.



Attribute Memory Read Timing Diagram

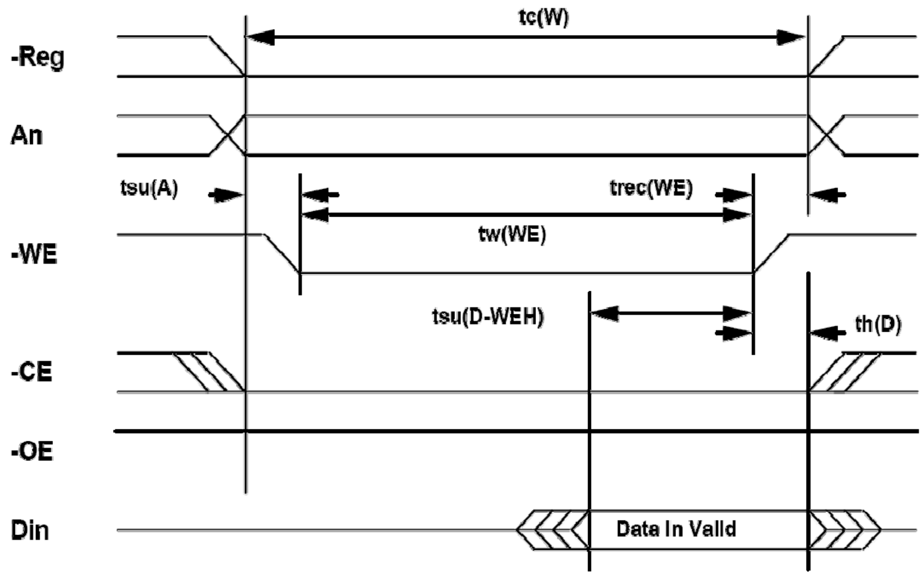
(2) Configuration Register (Attribute Memory) Write Timing Specification

The Card Configuration write access time is defined as 250 ns.

Speed Version			250 ns	
Item	Symbol	IEEE Symbol	Min ns.	Max ns.
Write Cycle Time	tc(W)	tAVAV	250	
Write Pulse Width	tw(WE)	tWLWH	150	
Address Setup Time	tsu(A)	tAVWL	30	
Write Recovery Time	trec(WE)	tWMAX	30	
Data Setup Time for WE	tsu(D-WEH)	tDVWH	80	
Data Hold Time	th(D)	tWMDX	30	

Note:

All times are in nanoseconds. Din signifies data provided by the system to the CompactFlash Storage Card or CF+ Card.



Configuration Register (Attribute Memory) Write Timing Diagram

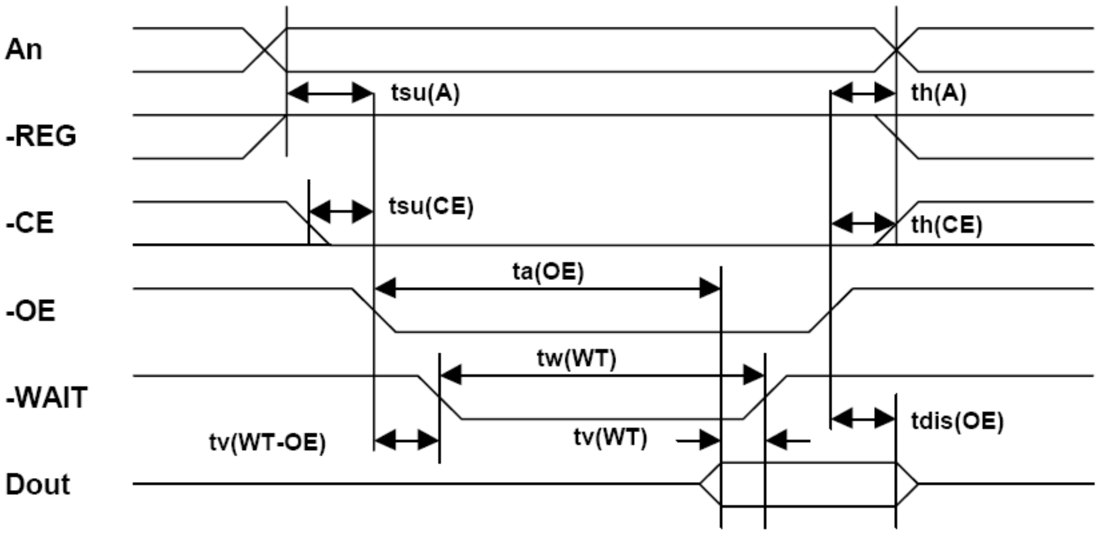
(3) Common Memory Read Timing Specification

Cycle Time Mode:			250 ns		120 ns		100 ns		80 ns	
Item	Symbol	IEEE Symbol	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.
Output Enable Access Time	ta(OE)	tGLQV		125		60		50		45
Output Disable Time from OE	Tdis (OE)	tGHQZ		100		60		50		45
Address Setup Time	tsu(A)	tAVGL	30		15		10		10	
Address Hold Time	th(A)	tGHAX	20		15		15		10	
CE Setup before OE	tsu(CE)	tELGL	0		0		0		0	
CE Hold following OE	th(CE)	tGHEH	20		15		15		10	
Wait Delay Falling from OE	tv(WT-OE)	tGLWTV		35		35		35		na[1]
Data Setup for Wait Release	tv(WT)	tQVWTH		0		0		0		na[1]
Wait Width Time[2]	tw(WT)	tWTLWTH		350 (3000 for CF+)		350 (3000 for CF+)		350 (3000 for CF+)		na[1]

Note:

1) –WAIT is not supported in this mode.

2) The maximum load on -WAIT is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Dout signifies data provided by the CompactFlash Storage Card or CF+Card to the system. The -WAIT signal may be ignored if the -OE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure. The Wait Width time meets the PCMCIA specification of 12µs but is intentionally less in this specification.

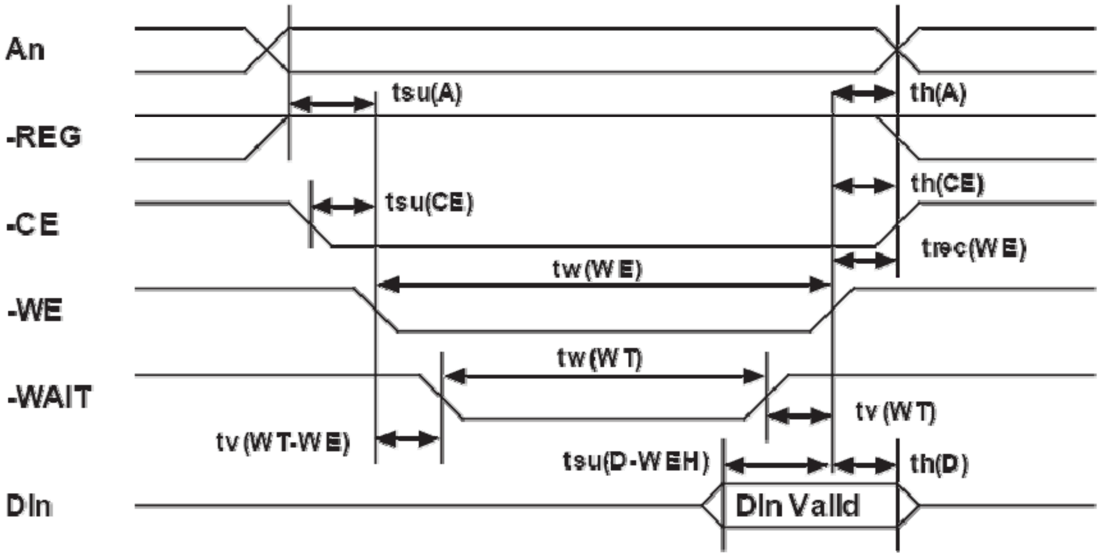


Common Memory Read Timing Diagram

(4) Common Memory Write Timing Specification

Cycle Time Mode:			250 ns		120 ns		100 ns		80 ns	
Item	Symbol	IEEE Symbol	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.
Data Setup before WE	tsu (D-WEH)	tDVWH	80		50		40		30	
Data Hold following WE	th (D)	tWMDX	30		15		10		10	
WE Pulse Width	tw (WE)	tWLWH	150		70		60		55	
Address Setup Time	tsu (A)	tAVWL	30		15		10		10	
CE Setup before WE	tsu (CE)	tELWL	0		0		0		0	
Write Recovery Time	trec (WE)	tWMAX	30		15		15		15	
Address Hold Time	th (A)	tGHAX	20		15		15		15	
CE Hold following WE	th (CE)	tGHEH	20		15		15		10	
Wait Delay Falling from WE	tv (WT-WE)	tWLWTV		35		35		35		na[1]
WE High from Wait Release	tv (WT)	tWTHWH	0		0		0		na[1]	
Wait Width Time[2]	tw (WT)	tWTLWTH		350 (3000 for CF+)		350 (3000 for CF+)		350 (3000 for CF+)		na[1]

Note:
1) –WAIT is not supported in this mode.
2) The maximum load on -WAIT is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Din signifies data provided by the system to the CompactFlash Storage Card. The -WAIT signal may be ignored if the -WE cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the Card Information Structure. The Wait Width time meets the PCMCIA specification of 12μs but is intentionally less in this specification.



Common Memory Write Timing Diagram

(5) I/O Input (Read) Timing Specification

Cycle Time Mode:			250 ns		120 ns		100 ns		80 ns	
Item	Symbol	IEEE Symbol	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.
Data Delay after IORD	td(IORD)	tlGLQV		100		50		45		45
Data Hold following IORD	th(IORD)	tlGHQX	0		5		5		5	
IORD Width Time	tw(IORD)	tlGLIGH	165		70		65		55	
Address Setup before IORD	tsuA(IORD)	tAVIGL	70		25		25		15	
Address Hold following IORD	thA(IORD)	tlGHAX	20		10		10		10	
CE Setup before IORD	tsuCE(IORD)	tELIGL	5		5		5		5	
CE Hold following IORD	thCE(IORD)	tlGHEH	20		10		10		10	
REG Setup before IORD	tsuREG(IORD)	tRGLIGL	5		5		5		5	
REG Hold following IORD	thREG(IORD)	tlGHRGH	0		0		0		0	
INPACK Delay Falling from IORD[3]	tdfINPACK(IORD)	tlGLIAL	0	45	0	na[1]	0	na[1]	0	na[1]
INPACK Delay Rising from IORD[3]	tdrINPACK(IORD)	tlGHIAH		45		na[1]		na[1]		na[1]
IOIS16 Delay Falling from Address[3]	tdfIOIS16 (ADR)	tAVISL		35		na[1]		na[1]		na[1]

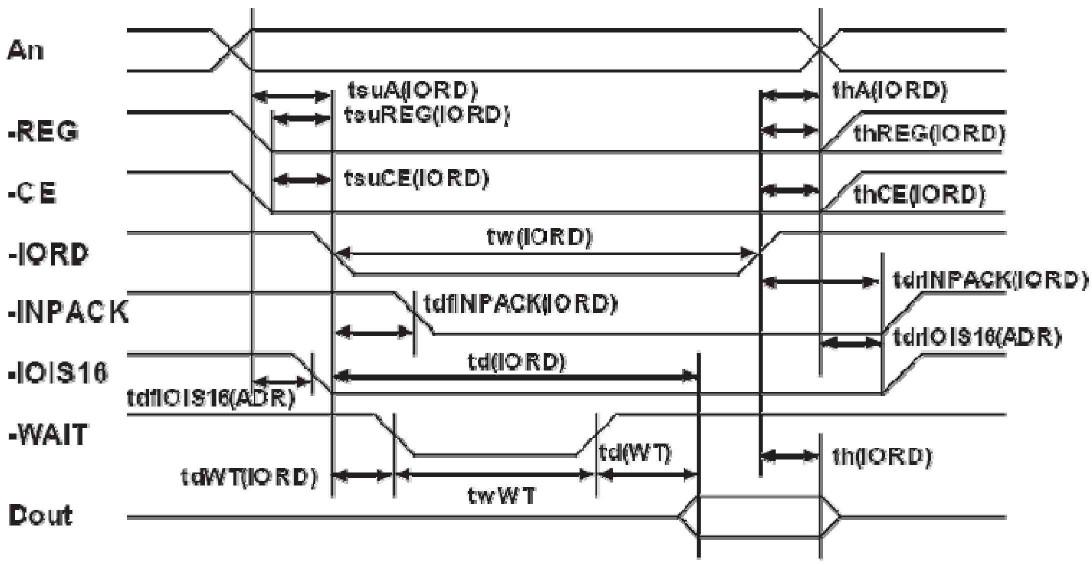
Item	Symbol	IEEE Symbol	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.
IOIS16 Delay Rising from Address[3]	tdrIOIS16 (ADR)	tAVISH		35		na[1]		na[1]		na[1]
Wait Delay Falling from IORD[3]	tdWT(IORD)	tIGLWTL		35		35		35		na[2]
Data Delay from Wait Rising[3]	td(WT)	tWTHQV		0		0		0		na[2]
Wait Width Time[3]	tw(WT)	tWTLWTH		350(3000 for CF+)		350(3000 for CF+)		350(3000 for CF+)		na[2]

Note:

1) -IOIS16 and -INPACK are not supported in this mode.

2) -WAIT is not supported in this mode.

3) Maximum load on -WAIT, -INPACK and -IOIS16 is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -WAIT high to -IORD high is 0 nsec, but minimum -IORD width shall still be met. Dout signifies data provided by the CompactFlash Storage Card or CF+ Card to the system. Wait Width time meets PCMCIA specification of 12µs but is intentionally less in this spec.



I/O Read Timing Diagram

(6) I/O Output (Write) Timing Specification

Cycle Time Mode:			250 ns		120 ns		100 ns		80 ns	
Item	Symbol	IEEE Symbol	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.
Data Setup before IOWR	tsu(IOWR)	tDVIWH	60		20		20		15	
Data Hold following IOWR	th(IOWR)	tlWHDX	30		10		5		5	
IOWR Width Time	tw(IOWR)	tlWLIWH	165		70		65		55	
Address Setup before IOWR	tsuA(IOWR)	tAVIWL	70		25		25		15	
Address Hold following IOWR	thA(IOWR)	tlWHAX	20		20		10		10	
CE Setup before IOWR	tsuCE(IOWR)	tELIWL	5		5		5		5	
CE Hold following IOWR	thCE(IOWR)	tlWHEH	20		20		10		10	
REG Setup before IOWR	tsuREG(IOWR)	tRGLIWL	5		5		5		5	
REG Hold following IOWR	thREG(IOWR)	tlWHRGH	0		0		0		0	
IOIS16 Delay Falling from Address[3]	tdfIOIS16(ADR)	tAVISL		35		na[1]		na[1]		na[1]
IOIS16 Delay Rising from Address[3]	tdrIOIS16(ADR)	tAVISH		35		na[1]		na[1]		na[1]
Wait Delay Falling from IOWR[3]	tdWT(IOWR)	tlWLWTL		35		35		35		na[2]

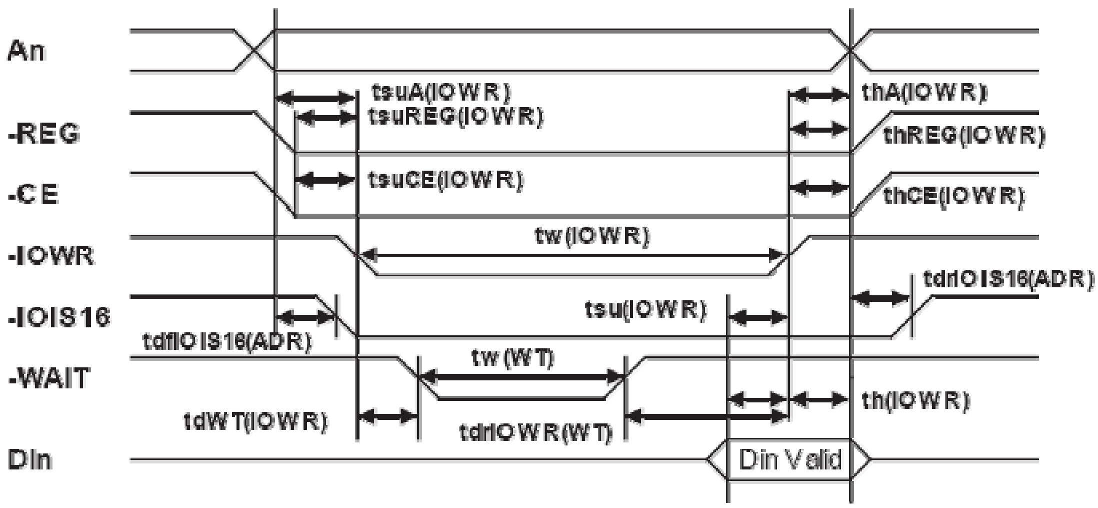
Item	Symbol	IEEE Symbol	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.	Min ns.	Max ns.
IOWR high from Wait high[3]	tdrIOWR(WT)	tWTJIWH	0		0		0		na[2]	
Wait Width Time[3]	tw(WT)	tWTLWTH		350(3000 for CF+)		350(3000 for CF+)		350(3000 for CF+)		na[2]

Note:

1) -IOIS16 and -INPACK are not supported in this mode.

2) -WAIT is not supported in this mode.

3) The maximum load on -WAIT, -INPACK, and -IOIS16 is 1 LSTTL with 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -WAIT high to -IOWR high is 0 nsec, but minimum -IOWR width shall still be met. Din signifies data provided by the system to the CompactFlash Storage Card or CF+ Card. The Wait Width time meets the PCMCIA specification of 12 µs but is intentionally less in this specification.



I/O Write Timing Diagram

(7) True IDE PIO Mode Read/Write Timing Specification

The timing diagram for True IDE mode of operation in this section is drawn using the conventions in the ATA-4 specification, which are different than the conventions used in the PCMCIA specification and earlier versions of this specification. Signals are shown with their asserted state as high regardless of whether the signal is actually negative or positive true. Consequently, the -IORD, the -IOWR and the -IOCS16 signals are shown in the diagram inverted from their electrical states on the bus.

	Item	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Note
t0	Cycle time (min)	600	383	240	180	120	100	80	1
t1	Address Valid to -IORD/-IOWR setup(min)	70	50	30	30	25	15	10	
t2	-IORD/-IOWR (min)	165	125	100	80	70	65	55	1
t2	-IORD/-IOWR (min)	290	290	290	80	70	65	55	1
t2i	Register (8 bit) -IORD/-IOWR	-	-	-	70	25	25	20	1
t3	recovery time (min)	60	45	30	30	20	20	15	
t4	-IOWR data setup(min)	30	20	15	10	10	5	5	
t5	-IOWR data hold(min)	50	35	20	20	20	15	10	
t6	-IORD data hold(min)	5	5	5	5	5	5	5	
t6Z	-IORD data tristate(max)	30	30	30	30	30	20	20	2
t7	Address valid to -IOCS16 assertion(max)	90	50	40	n/a	n/a	n/a	n/a	4
t8	Address valid to -IOCS16 released(max)	60	45	30	n/a	n/a	n/a	n/a	4
	Item	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Note
t9	-IORD/-IOWR to address valid hold	20	15	10	10	10	10	10	
tRD	Read Data Valid to IORDY active (min), if IORDY initially low after tA	0	0	0	0	0	0	0	
tA	IORDY Setup time	35	35	35	35	35	na[5]	na[5]	3
tB	IORDY Pulse Width(max)	1250	1250	1250	1250	1250	na[5]	na[5]	
tC	IORDY assertion torelease (max)	5	5	5	5	5	na[5]	na[5]	

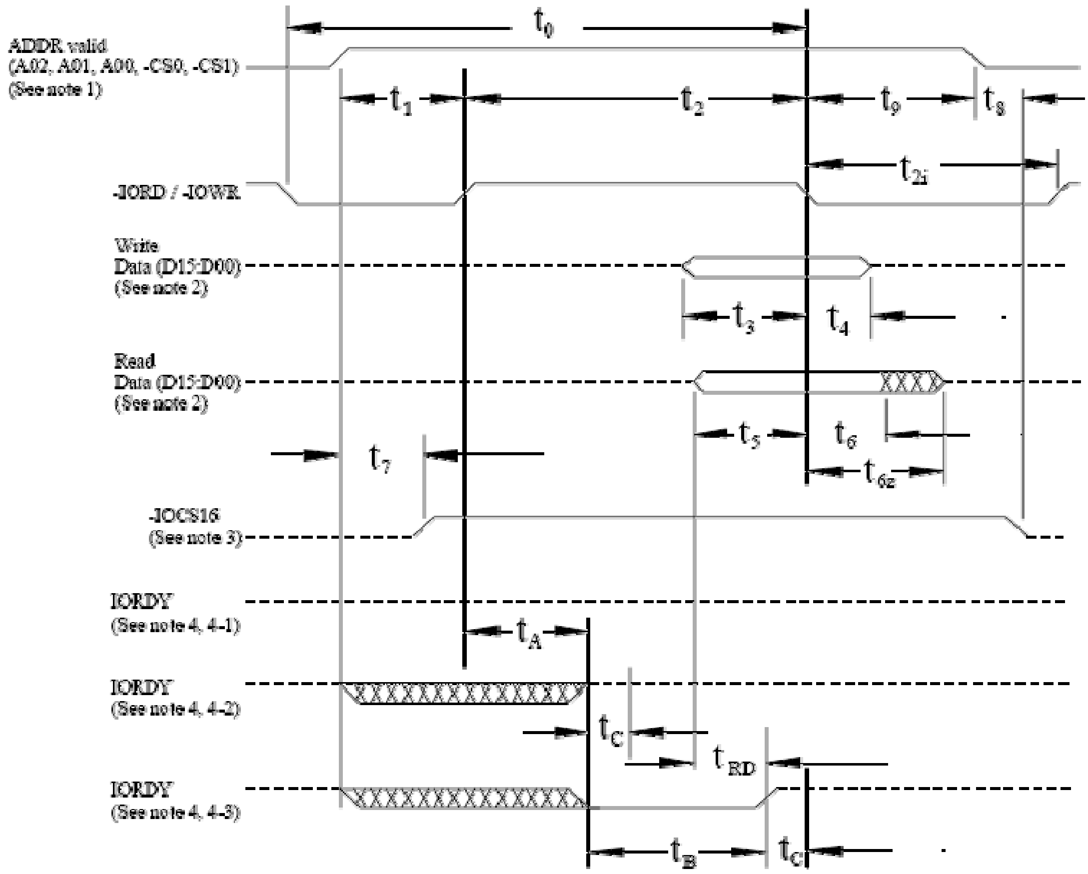
Note:
All timings are in nanoseconds. The maximum load on -IOCS16 is 1 LSTTL with a 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from -IORDY high to -IORD high is 0 nsec, but minimum -IORD width shall still be met.

1) t0 is the minimum total cycle time, t2 is the minimum command active time, and t2i is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, t2, and t2i shall be met. The minimum total cycle time requirement is greater than the sum of t2 and t2i. This means a host implementation can lengthen either or both t2 or t2i to ensure that t0 is equal to or greater than the value reported in the device's identify device data. A CompactFlash Storage Card implementation shall support any legal host implementation.

2) This parameter specifies the time from the negation edge of -IORD to the time that the data bus is no longer driven by the CompactFlash Storage Card (tri-state).
3) The delay from the activation of -IORD or -IOWR until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the PIO cycle can be completed. If the CompactFlash Storage Card is not driving IORDY negated at tA after the activation of -IORD or -IOWR, then t5 shall be met and tRD is not applicable. If the CompactFlash Storage Card is driving IORDY negated at the time tA after the activation of -IORD or -IOWR, then tRD shall be met and t5 is not applicable.

4) t7 and t8 apply only to modes 0, 1 and 2. For other modes, this signal is not valid.

5) IORDY is not supported in this mode.



True IDE PIO Mode Timing Diagram

Note:
(1) Device address consists of -CS0, -CS1, and A[02::00]
(2) Data consists of D[15::00] (16-bit) or D[07::00] (8 bit)

(3) -IOCS16 is shown for PIO modes 0, 1 and 2. For other modes, this signal is ignored.
(4) The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after tA from the assertion of -IORD or -IOWR. The assertion and negation of IORDY is described in the following three cases:
(4-1) Device never negates IORDY: No wait is generated.
(4-2) Device starts to drive IORDY low before tA, but causes IORDY to be asserted before tA: No wait generated.
(4-3) Device drives IORDY low before tA: wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and -IORD is asserted, the device shall place read data on D15-D00 for tRD before causing IORDY to be asserted.

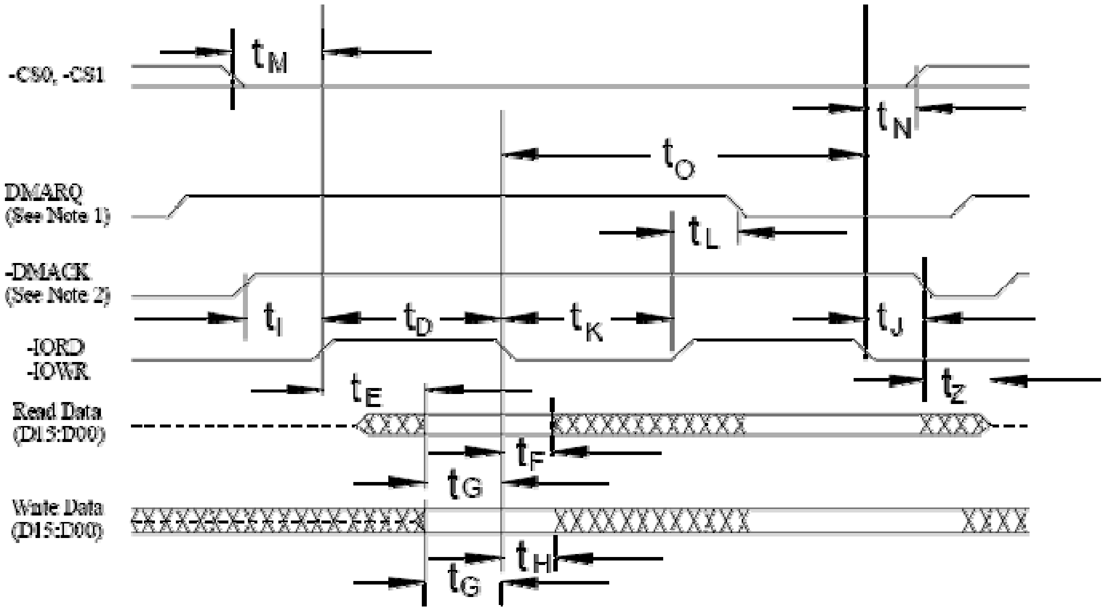
(8) True IDE Multiword DMA Mode Read/Write Timing Specification

The timing diagram for True IDE DMA mode of operation in this section is drawn using the conventions in the ATA-4 specification, which are different than the conventions used in the PCMCIA specification and earlier versions of this specification. Signals are shown with their asserted state as high regardless of whether the signal is actually negative or positive true. Consequently, the -IORD, the -IOWR and the -IOCS16 signals are shown in the diagram inverted from their electrical states on the bus.

	Item	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Note
t_O	Cycle time (min)	480	150	120	100	80	1
t_D	-IORD / -IOWR asserted width(min)	215	80	70	65	55	1
t_E	-IORD data access (max)	150	60	50	50	45	
t_F	-IORD data hold (min)	5	5	5	5	5	
t_G	-IORD/-IOWR data setup (min)	100	30	20	15	10	
t_H	-IOWR data hold (min)	20	15	10	5	5	
t_I	DMACK to –IORD/-IOWR setup(min)	0	0	0	0	0	
t_J	-IORD / -IOWR to -DMACK hold(min)	20	5	5	5	5	
t_{KR}	-IORD negated width (min)	50	50	25	25	20	1
t_{KW}	-IOWR negated width (min)	215	50	25	25	20	1
t_{LR}	-IORD to DMARQ delay (max)	120	40	35	35	35	
t_{LW}	-IOWR to DMARQ delay (max)	40	40	35	35	35	
t_M	CS(1:0) valid to –IORD / -IOWR	50	30	25	10	5	
t_N	CS(1:0) hold	15	10	10	10	10	
t_Z	-DMACK	20	25	25	25	25	

Notes:

1) *t0 is the minimum total cycle time and tD is the minimum command active time, while tKR and tKW are the minimum command recovery time or command inactive time for input and output cycles respectively. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t0, tD, tKR, and tKW shall be met. The minimum total cycle time requirement is greater than the sum of tD and tKR or tKW.for input and output cycles respectively. This means a host implementation can lengthen either or both of tD and either of tKR, and tKW as needed to ensure that t0 is equal to or greater than the value reported in the device's identify device data. A CompactFlash Storage Card implementation shall support any legal host implementation.*



True IDE Multiword DMA Mode Read/Write Timing Diagram

Notes:

(1) If the Card cannot sustain continuous, minimum cycle time DMA transfers, it may negate DMARQ within the time specified from the start of a DMA transfer cycle to suspend the DMA transfers in progress and reassert the signal at a later time to continue the DMA operation.

(2) This signal may be negated by the host to suspend the DMA transfer in progress.

(9) True IDE Ultra DMA Mode Read/Write Timing Specification

1) Ultra DMA Overview

Ultra DMA is an optional data transfer protocol used with the READ DMA, and WRITE DMA, commands. When this protocol is enabled, the Ultra DMA protocol shall be used instead of the Multiword DMA protocol when these commands are issued by the host. This protocol applies to the Ultra DMA data burst only. When this protocol is used there are no changes to other elements of the ATA protocol (e.g., Command Block Register access).

Several signal lines are redefined to provide different functions during an Ultra DMA burst. These lines assume these definitions when:

1. an Ultra DMA mode is selected, and
2. a host issues a READ DMA, or a WRITE DMA command requiring data transfer, and
3. the host asserts -DMACK.

These signal lines revert back to the definitions used for non-Ultra DMA transfers upon the negation of -DMACK by the host at the termination of an Ultra DMA burst.

With the Ultra DMA protocol, the STROBE signal that latches data from D[15:00] is generated by the same agent (either host or device) that drives the data onto the bus. Ownership of D[15:00] and this data strobe signal are given either to the device during an Ultra DMA data-in burst or to the host for an Ultra DMA data-out burst.

With the Ultra DMA protocol, the STROBE signal that latches data from D[15:00] is generated by the same agent (either host or device) that drives the data onto the bus. Ownership of D[15:00] and this data strobe signal are given either to the device during an Ultra DMA data-in burst or to the host for an Ultra DMA data-out burst.

During an Ultra DMA burst a sender shall always drive data onto the bus, and, after a sufficient time to allow for propagation delay, cable settling, and setup time, the sender shall generate a STROBE edge to latch the data. Both edges of STROBE are used for data transfers so that the frequency of STROBE is limited to the same frequency as the data.

Words in the IDENTIFY DEVICE data indicate support of the Ultra DMA feature and the Ultra DMA modes the device is capable of supporting. The Set transfer mode subcommand in the SET FEATURES command shall be used by a host to select the Ultra DMA mode at which the system operates. The Ultra DMA mode selected by a host shall be less than or equal to the fastest mode of which the device is capable. Only one Ultra DMA mode shall be selected at any given time. All timing requirements for a selected Ultra DMA mode shall be satisfied. Devices supporting any Ultra DMA mode shall also support all slower Ultra DMA modes.

An Ultra DMA capable device shall retain the previously selected Ultra DMA mode after executing a software reset sequence or the sequence caused by receipt of a DEVICE RESET command if a SET FEATURES disable reverting to defaults command has been issued. The device may revert to a Multiword DMA mode if a SET FEATURES enable reverting to default has been issued. An Ultra DMA capable device shall clear any previously selected Ultra DMA mode and revert to the default non-Ultra DMA modes after executing a power-on or hardware reset.

Both the host and device perform a CRC function during an Ultra DMA burst. At the end of an Ultra DMA burst the host sends its CRC data to the device. The device compares its CRC data to the data sent from the host. If the two values do not match, the device reports an error in the error register. If an error occurs during one or more Ultra DMA bursts for any one command, the device shall report the first error that occurred. If the device detects that a CRC error has occurred before data transfer for the command is complete, the device may complete the transfer and report the error or abort the command and report the error.

NOTE:

If a data transfer is terminated before completion, the assertion of INTRQ should be passed through to the host software driver regardless of whether all data requested by the command has been transferred.

2) Ultra DMA Phases of Operation

An Ultra DMA data transfer is accomplished through a series of Ultra DMA data-in or data-out bursts. Each Ultra DMA burst has three mandatory phases of operation: the initiation phase, the data transfer phase, and the Ultra DMA burst termination phase. In addition, an Ultra DMA burst may be paused during the data transfer phase (see: 14.3.18.3 Ultra DMA Data Transfer, for the detailed protocol descriptions for each of these phases. Table 22: Ultra DMA Data Burst Timing Requirements and Table 23: Ultra DMA Data Burst Timing Descriptions define the specific timing requirements). In the following rules -DMARDY is used in cases that could apply to either -DDMARDY or -HDMARDY, and STROBE is used in cases that could apply to either DSTROBE or HSTROBE. The following are general Ultra DMA rules.

1. An Ultra DMA burst is defined as the period from an assertion of -DMACK by the host to the subsequent negation of -DMACK.
2. When operating in Ultra DMA modes 2, 1, or 0 a recipient shall be prepared to receive up to two data words whenever an Ultra DMA burst is paused. When operating in Ultra DMA modes 6, 5, 4, or 3 a recipient shall be prepared to receive up to three data words whenever an Ultra DMA burst is paused.

3) Ultra DMA Burst Initiation Phase Rules

1. An Ultra DMA burst initiation phase begins with the assertion of DMARQ by a device and ends when the sender generates a STROBE edge to transfer the first data word.
2. An Ultra DMA burst shall always be requested by a device asserting DMARQ.
3. When ready to initiate the requested Ultra DMA burst, the host shall respond by asserting -DMACK.
4. A host shall never assert -DMACK without first detecting that DMARQ is asserted.
5. For Ultra DMA data-in bursts: a device may begin driving D[15:00] after detecting that -DMACK is asserted, STOP negated, and -HDMARDY is asserted.
6. After asserting DMARQ or asserting -DDMARDY for an Ultra DMA data-out burst, a device shall not negate either signal until the first STROBE edge is generated.
7. After negating STOP or asserting -HDMARDY for an Ultra DMA data-in burst, a host shall not change the state of either signal until the first STROBE edge is generated.

4) Ultra DMA Data transfer phase rules

1. The data transfer phase is in effect from after Ultra DMA burst initiation until Ultra DMA burst termination.
2. A recipient pauses an Ultra DMA burst by negating -DMARDY and resumes an Ultra DMA burst by reasserting -DMARDY.
3. A sender pauses an Ultra DMA burst by not generating STROBE edges and resumes by generating STROBE edges.
4. A recipient shall not signal a termination request immediately when the sender stops generating STROBE edges. In the absence of a termination from the sender the recipient shall always negate -DMARDY and wait the required period before signaling a termination request.
5. A sender may generate STROBE edges at greater than the minimum period specified by the enabled Ultra DMA mode. The sender shall not generate STROBE edges at less than the minimum period specified by the enabled Ultra DMA mode. A recipient shall be able to receive data at the minimum period specified by the enabled Ultra DMA mode.

5) Ultra DMA Burst Termination Phase Rules

1. Either a sender or a recipient may terminate an Ultra DMA burst.
2. Ultra DMA burst termination is not the same as command completion. If an Ultra DMA burst termination occurs before command completion, the command shall be completed by initiation of a new Ultra DMA burst at some later time or aborted by the host issuing a hardware or software reset or DEVICE RESET command if implemented by the device.
3. An Ultra DMA burst shall be paused before a recipient requests a termination.
4. A host requests a termination by asserting STOP. A device acknowledges a termination request by negating DMARQ.
5. A device requests a termination by negating DMARQ. A host acknowledges a termination request by asserting STOP.
6. Once a sender requests a termination, the sender shall not change the state of STROBE until the recipient acknowledges the request. Then, if STROBE is not in the asserted state, the sender shall return STROBE to the asserted state. No data shall be transferred on this transition of STROBE.
7. A sender shall return STROBE to the asserted state whenever the sender detects

a termination request from the recipient. No data shall be transferred nor CRC calculated on this edge of DSTROBE.

8. Once a recipient requests a termination, the responder shall not change DMARDY from the negated state for the remainder of an Ultra DMA burst.
9. A recipient shall ignore a STROBE edge when DMARQ is negated or STOP is asserted.

6) Ultra DMA Data Transfers Timing

Ultra DMA Data Burst Timing Requirements

Name	UDMA Mode 0		UDMA Mode 1		UDMA Mode 2		UDMA Mode 3		UDMA Mode 4		Measurement location (See Note 2)
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{2CYCTYP}$	240		160		120		90		60		Sender
t_{CYC}	112		73		54		39		25		Note 3
t_{2CYC}	230		153		115		86		57		Sender
t_{DS}	15.0		10.0		7.0		7.0		5.0		Recipient
t_{DH}	5.0		5.0		5.0		5.0		5.0		Recipient
t_{DVS}	70.0		48.0		31.0		20.0		6.7		Sender
t_{DVH}	6.2		6.2		6.2		6.2		6.2		Sender
t_{CS}	15.0		10.0		7.0		7.0		5.0		Device
t_{CH}	5.0		5.0		5.0		5.0		5.0		Device
t_{CVS}	70.0		48.0		31.0		20.0		6.7		Host
t_{CVH}	6.2		6.2		6.2		6.2		6.2		Host
t_{ZFS}	0		0		0		0		0		Device
t_{DZFS}	70.0		48.0		31.0		20.0		6.7		Sender
t_{FS}		230		200		170		130		120	Device
t_{LI}	0	150	0	150	0	150	0	100	0	100	Note 4
t_{MLI}	20		20		20		20		20		Host
t_{UI}	0		0		0		0		0		Host
t_{AZ}		10		10		10		10		10	Note 5
t_{ZAH}	20		20		20		20		20		Host
t_{ZAD}	0		0		0		0		0		Device
t_{ENV}	20	70	20	70	20	70	20	55	20	55	Host
t_{RFS}		75		70		60		60		60	Sender

t_{RP}	160		125		100		100		100		Recipient
t_{IORDYZ}		20		20		20		20		20	Device
t_{ZIORDY}	0		0		0		0		0		Device
t_{ACK}	20		20		20		20		20		Host
t_{SS}	50		50		50		50		50		Sender

Notes:

1) All timing measurement switching points (low to high and high to low) shall be taken at 1.5 V.

2) All signal transitions for a timing parameter shall be measured at the connector specified in the measurement location column. For example, in the case of tRFS, both STROBE and -DMARDY transitions are measured at the sender connector.

3) The parameter tCYC shall be measured at the recipient's connector farthest from the sender.

4) The parameter tLI shall be measured at the connector of the sender or recipient that is responding to an incoming transition from the recipient or sender respectively. Both the incoming signal and the outgoing response shall be measured at the same connector.

5)The parameter tAZ shall be measured at the connector of the sender or recipient that is driving the bus but must release the bus the allow for a bus turnaround.

6) See the AC Timing requirements in Table 25: Ultra DMA AC Signal Requirements.

Ultra DMA Data Burst Timing Descriptions

Name	Comment	Note
$t_{2CYCTYP}$	Typical sustained average two cycle time	
t_{CYC}	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)	
Name	Comment	Note
t_{2CYC}	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)	
t_{DS}	Data setup time at recipient (from data valid until STROBE edge)	2, 5
t_{DH}	Data hold time at recipient (from STROBE edge until data may become invalid)	2, 5
t_{DVS}	Data valid setup time at sender (from data valid until STROBE edge)	3
t_{DVH}	Data valid hold time at sender (from STROBE edge until data may become invalid)	3
t_{CS}	CRC word setup time at device	2
t_{CH}	CRC word hold time device	2

t_{CVS}	CRC word valid setup time at host (from CRC valid until -DMACK negation)	3
t_{CVH}	CRC word valid hold time at sender (from -DMACK negation until CRC may become invalid)	3
t_{ZFS}	Time from STROBE output released-to-driving until the first transition of critical timing.	
t_{DZFS}	Time from data output released-to-driving until the first transition of critical timing.	
t_{FS}	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)	
t_{LI}	Limited interlock time	1
t_{MLI}	Interlock time with minimum	1
t_{UI}	Unlimited interlock time	1
t_{AZ}	Maximum time allowed for output drivers to release (from asserted or negated)	
t_{ZAH}	Minimum delay time required for output	
t_{ZAD}	drivers to assert or negate (from released)	
t_{ENV}	Envelope time (from -DMACK to STOP and -HDMARDY during data in burst initiation and from DMACK to STOP during data out burst initiation)	
t_{RFS}	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of -DMARDY)	
Name	Comment	Note
t_{RP}	Ready-to-pause time (that recipient shall wait to pause after negating -DMARDY)	
t_{IORDYZ}	Maximum time before releasing IORDY	
t_{ZIORDY}	Minimum time before driving IORDY	4
t_{ACK}	Setup and hold times for -DMACK (before assertion or negation)	
t_{SS}	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)	

Notes:

1) The parameters t_{UI}, t_{MLI} (in Figure Ultra DMA Data-In Burst Device Termination Timing and Figure Ultra DMA Data-In Burst Host Termination Timing), and t_{LI} indicate sender-to-recipient or recipient-to-sender interlocks, i.e., one agent (either sender or recipient) is waiting for the other agent to respond with a signal before proceeding. t_{UI} is an unlimited interlock that has no maximum time value. t_{MLI} is a limited time-out that has a defined minimum. t_{LI} is a limited time-out that has a defined maximum.

2) 80-conductor cabling (see 4.3.8.4) shall be required in order to meet setup (t_{DS}, t_{CS}) and hold (t_{DH}, t_CH) times in modes greater than 2.

3) Timing for t_{DVS}, t_{DVH}, t_{CVS} and t_{CVH} shall be met for lumped capacitive loads of 15 and 40 pF at the connector where the Data and STROBE signals have the same capacitive load value. Due to reflections on the cable, these timing measurements are not valid in a normally functioning system.

4) For all modes the parameter t_{ZIORDY} *may be greater than* t_{ENV} *due to the fact that the host has a pull-up on IORDY- giving it a known state when released.*

5) The parameters t_{DS}*, and* t_{DH} *for mode 5 are defined for a recipient at the end of the cable only in a configuration with a single device located at the end of the cable. This could result in the minimum values for* t_{DS} *and* t_{DH} *for mode 5 at the middle connector being 3.0 and 3.9 ns respectively.*

Ultra DMA Sender and Recipient IC Timing Requirements

Name	Comments	UDMA Mode 0		UDMA Mode 1		UDMA Mode 2		UDMA Mode 3		UDMA Mode 4	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
t_{DSIC}	Recipient IC data setup time (from data valid until STROBE edge) (see note 2)	14.7		9.7		6.8		6.8		4.8	
t_{DHIC}	Recipient IC data hold time (from STROBE edge until data may become invalid) (see note 2)	4.8		4.8		4.8		4.8		4.8	

Name	Comments	UDMA Mode 0		UDMA Mode 1		UDMA Mode 2		UDMA Mode 3		UDMA Mode 4	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
t_{DVSIC}	Sender IC data valid setup time (from data valid until STROBE edge) (see note 3)	72.9		50.9		33.9		22.6		9.5	
t_{DVHIC}	Sender IC data valid hold time (from STROBE edge until data may become invalid) (see note 3)	9.0		9.0		9.0		9.0		9.0	

Notes:

1) All timing measurement switching points(low to high and high to low) shall be taken at 1.5 V.

2) The correct data value shall be captured by the recipient given input data with a slew rate of 0.4 V/ns rising and falling and the input STROBE with a slew rate of 0.4 V/ns rising and falling at tDSIC and tDHIC timing (as measured through 1.5 V).

3) The parameters tDVSIC and tDVHIC shall be met for lumped capacitive loads of 15 and 40 pF at the IC where all signals have the same capacitive load value. Noise that may couple onto the output signals from external sources has not been included in these values.

Ultra DMA AC Signal Requirements

Name	Comment	Min [V/ns]	Max [V/ns]	Notes
S_{RISE}	Rising Edge Slew Rate for any signal		1.25	1
S_{FALL}	Falling Edge Slew Rate for any signal		1.25	1

Note:

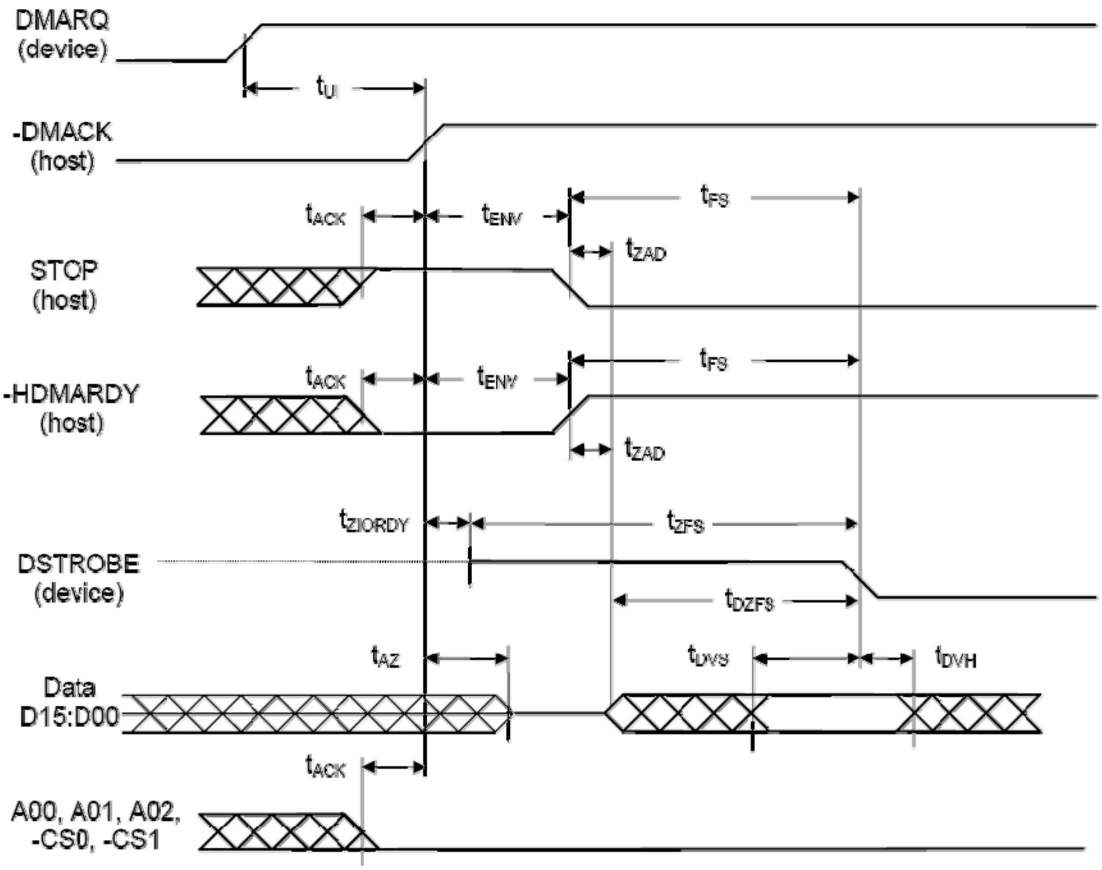
1) The sender shall be tested while driving an 18 inch long, 80 conductor cable with PVC insulation material. The signal under test shall be cut at a test point so that it has not trace, cable or recipient loading after the test point. All other signals should remain connected through to the recipient. The test point may be located at any point between the sender's series termination resistor and one half inch or less of conductor exiting the connector. If the test point is on a cable conductor rather than the PCB, an adjacent ground conductor shall also be cut within one half inch of the connector.

The test load and test points should then be soldered directly to the exposed source side connectors. The test loads consist of a 15 pF or a 40 pF, 5%, 0.08 inch by 0.05 inch surface mount or smaller size capacitor from the test point to ground. Slew rates shall be met for both capacitor values.

Measurements shall be taken at the test point using a <1 pF, >100 Kohm, 1 Ghz or faster probe and a 500 MHz or faster oscilloscope. The average rate shall be measured from 20% to 80% of the settled VOH level with data transitions at least 120 nsec apart. The settled VOH level shall be measured as the average output high level under the defined testing conditions from 100 nsec after 80% of a rising edge until 20% of the subsequent falling edge.

Initiating an Ultra DMA Data-In Burst

a. An Ultra DMA Data-In burst is initiated by following the steps lettered below. The timing diagram is shown in Figure 33: Ultra DMA Data-In Burst Initiation Timing. The associated timing parameters are specified in Table 22: Ultra DMA Data Burst Timing Requirements and are described in Table 23: Ultra DMA Data Burst Timing Descriptions.
b. The following steps shall occur in the order they are listed unless otherwise specifically allowed:
c. The host shall keep -DMACK in the negated state before an Ultra DMA burst is initiated.
d. The device shall assert DMARQ to initiate an Ultra DMA burst. After assertion of DMARQ the device shall not negate DMARQ until after the first negation of DSTROBE.
e. Steps (c), (d), and (e) may occur in any order or at the same time. The host shall assert STOP.
f. The host shall negate -HDMARDY.
g. The host shall negate -CS0, -CS1, DA2, DA1, and DA0. The host shall keep -CS0, -CS1, DA2, DA1, and DA0 negated until after negating -DMACK at the end of the burst.
h. Steps (c), (d), and (e) shall have occurred at least tACK before the host asserts -DMACK. The host shall keep -DMACK asserted until the end of an Ultra DMA burst.
i. The host shall release D[15:00] within tAZ after asserting -DMACK.
j. The device may assert DSTROBE tZIORDY after the host has asserted -DMACK. Once the device has driven DSTROBE the device shall not release DSTROBE until after the host has negated -DMACK at the end of an Ultra DMA burst.
k. The host shall negate STOP and assert -HDMARDY within tENV after asserting -DMACK. After negating STOP and asserting -HDMARDY, the host shall not change the state of either signal until after receiving the first transition of DSTROBE from the device (i.e., after the first data word has been received).
l. The device shall drive D[15:00] no sooner than tZAD after the host has asserted -DMACK, negated STOP, and asserted -HDMARDY. m) The device shall drive the first word of the data transfer onto D[15:00]. This step may occur when the device first drives D[15:00] in step (j).
m. To transfer the first word of data the device shall negate DSTROBE within tFS after the host has negated STOP and asserted -HDMARDY. The device shall negate DSTROBE no sooner than tDVS after driving the first word of data onto D[15:00].



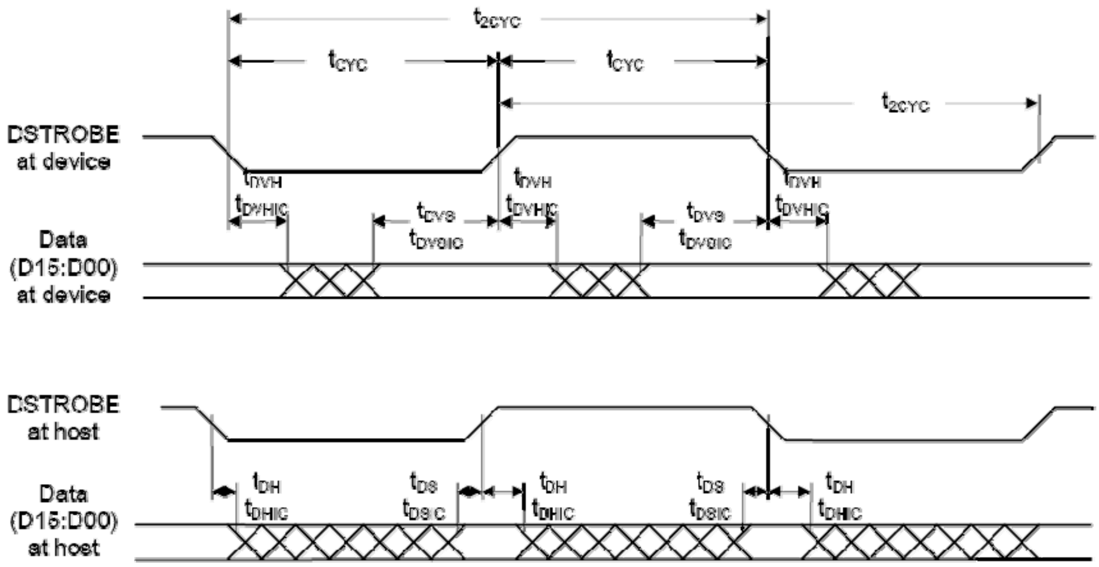
Notes:

The definitions for the IORDY:-DDMARDY:DSTROBE, -IORD: -HDMARDY:HSTROBE, and -IOWR:STOP signal lines are not in effect until DMARQ and -DMACK are asserted.

Sustaining an Ultra DMA Data-In Burst

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a. The device shall drive a data word onto D[15:00].
b. The device shall generate a DSTROBE edge to latch the new word no sooner than tDVS after changing the state of D[15:00]. The device shall generate a DSTROBE edge no more frequently than tCYC for the selected Ultra DMA mode. The device shall not generate two rising or two falling DSTROBE edges more frequently than 2tcyc for the selected Ultra DMA mode.
c. The device shall not change the state of D[15:00] until at least tDVH after generating a DSTROBE edge to latch the data.
d. The device shall repeat steps (a), (b), and (c) until the data transfer is complete or an Ultra DMA burst is paused, whichever occurs first.



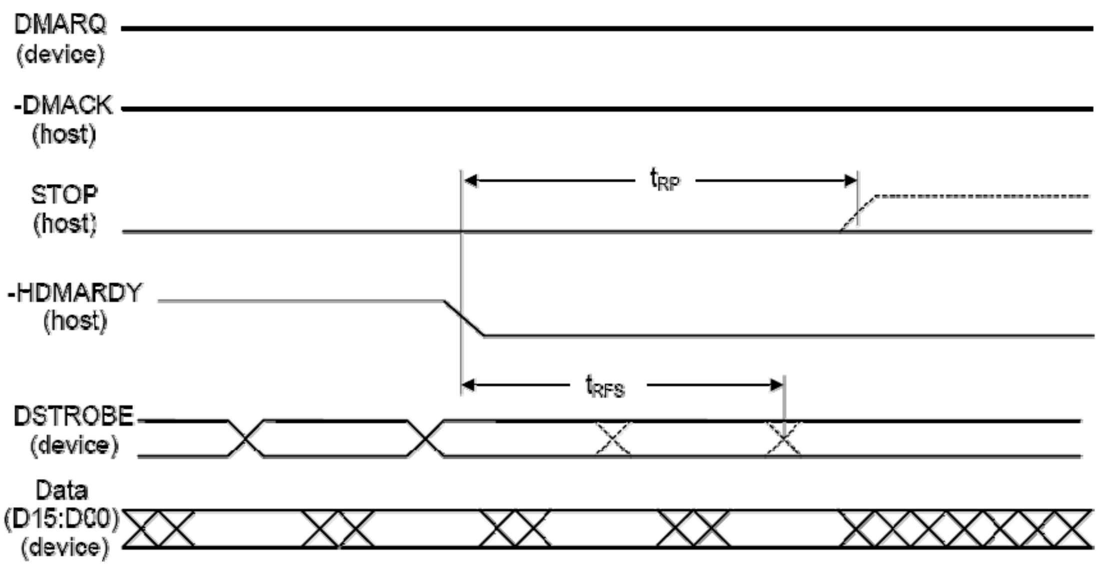
Notes:

D[15:00] and DSTROBE signals are shown at both the host and the device to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the host until some time after they are driven by the device.

Host Pausing an Ultra DMA Data-In Burst

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a. The host shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.
b. The host shall pause an Ultra DMA burst by negating -HDMARDY.
c. The device shall stop generating DSTROBE edges within tRFS of the host negating -HDMARDY.
d. If the host negates -HDMARDY within tSR after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero or one additional data words. If the host negates -HDMARDY greater than tSR after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero, one or two additional data words. The additional data words are a result of cable round trip delay and tRFS timing for the device.
e. The host shall resume an Ultra DMA burst by asserting -HDMARDY.



Notes:

1) The host may assert STOP to request termination of the Ultra DMA burst no sooner than tRP after -HDMARDY is negated.

2) After negating -HDMARDY, the host may receive zero, one, two, or three more data words from the device.

Device Terminating an Ultra DMA Data-In Burst

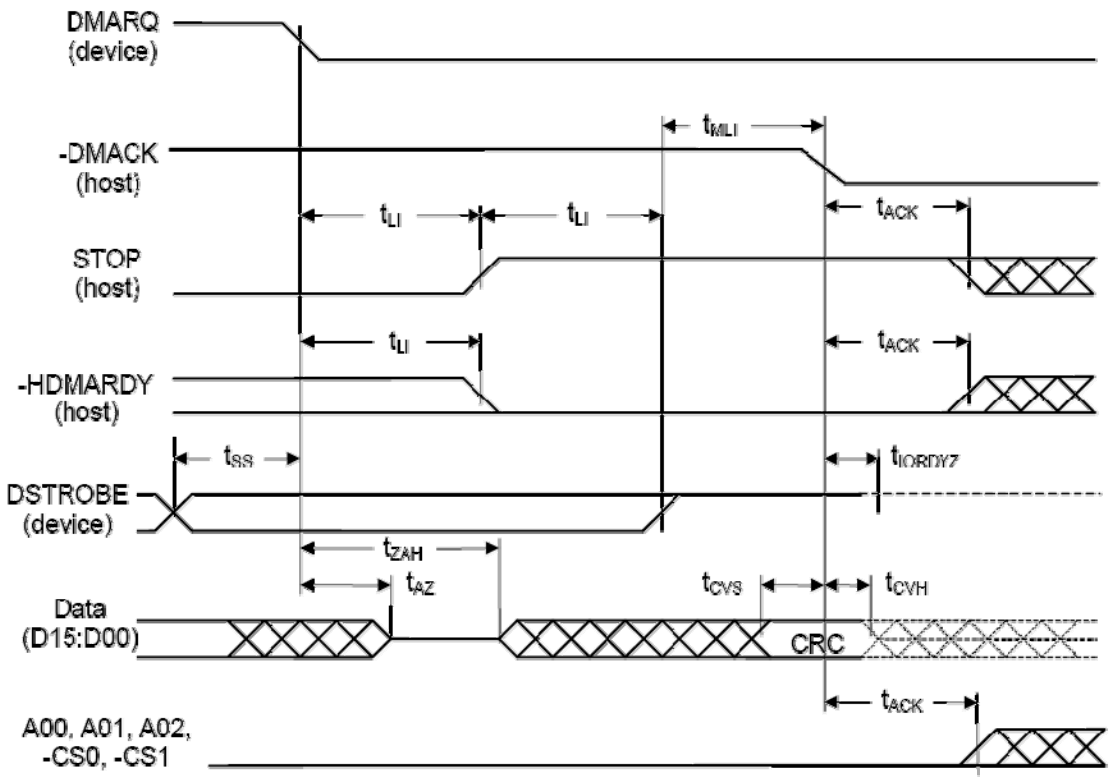
The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a. The device shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.

b. The device shall pause an Ultra DMA burst by not generating DSTROBE edges.

c. NOTE − The host shall not immediately assert STOP to initiate Ultra DMA burst termination when the device stops generating STROBE edges. If the device does not negate DMARQ, in order to initiate ULTRA DMA burst termination, the host shall negate -HDMARDY and wait tRP before asserting STOP.

d. The device shall resume an Ultra DMA burst by generating a DSTROBE edge.



Notes:

The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

Host Terminating an Ultra DMA Data-In Burst

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a. The host shall not initiate Ultra DMA burst termination until at least one data word of an Ultra DMA burst has been transferred.

b. The host shall initiate Ultra DMA burst termination by negating -HDMARDY. The host shall continue to negate -HDMARDY until the Ultra DMA burst is terminated.

c. The device shall stop generating DSTROBE edges within tRFS of the host negating HDMARDY

d. If the host negates -HDMARDY within tSR after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero or one additional data words. If the host negates HDMARDYgreater than tSR after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero, one or two additional data words. The additional data words are a result of cable round trip delay and tRFS timing for the device.

e. The host shall assert STOP no sooner than tRP after negating -HDMARDY. The host shall not negate STOP again until after the Ultra DMA burst is terminated.

f. The device shall negate DMARQ within tLI after the host has asserted STOP. The device shall not assert DMARQ again until after the Ultra DMA burst is terminated.

g. If DSTROBE is negated, the device shall assert DSTROBE within tLI after the host has asserted STOP. No data shall be transferred during this assertion. The host shall ignore this transition on DSTROBE. DSTROBE shall remain asserted until the Ultra DMA burst is terminated.

h. The device shall release D[15:00] no later than t AZ after negating DMARQ.

i. The host shall drive DD D[15:00] no sooner than tZAH after the device has negated DMARQ. For this step, the host may first drive D[15:00] with the result of its CRC calculation .

j. If the host has not placed the result of its CRC calculation on D[15:00] since first driving D[15:00] during (9), the host shall place the result of its CRC calculation on D[15:00].

k. The host shall negate -DMACK no sooner than tMLI after the device has asserted DSTROBE and negated DMARQ and the host has asserted STOP and negated HDMARDY, and no sooner than tDVS after the host places the result of its CRC calculation on D[15:00].

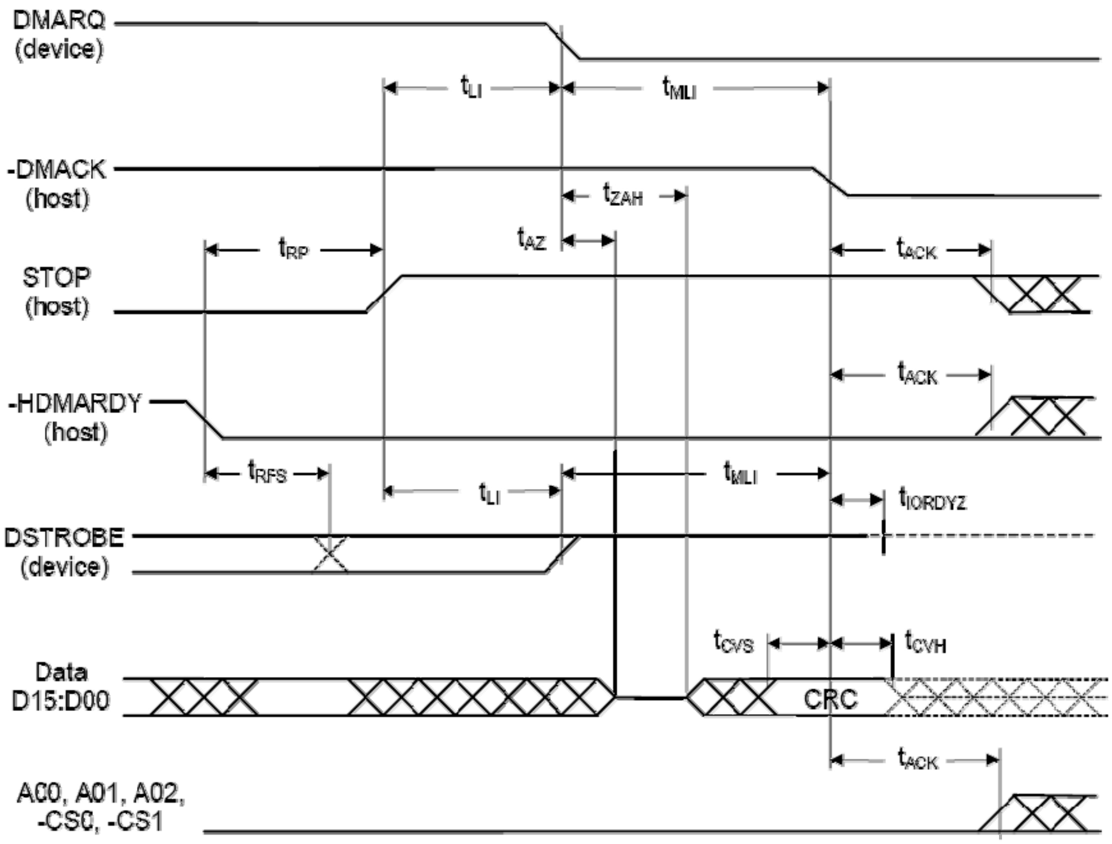
l. The device shall latch the host's CRC data from D[15:00] on the negating edge of DMACK.

m. The device shall compare the CRC data received from the host with the results of its own CRC calculation. If a miscompare error occurs during one or more Ultra DMA burst for any one command, at the end of the command, the device shall report the first error that occurred.

n. The device shall release DSTROBE within tIORDYZ after the host negates -DMACK.

o. The host shall neither negate STOP nor assert -HDMARDY until at least tACK after the host has negated -DMACK.

p. The host shall not assert -IORD, -CS0, -CS1, DA2, DA1, or DA0 until at least tACK after negating DMACK.



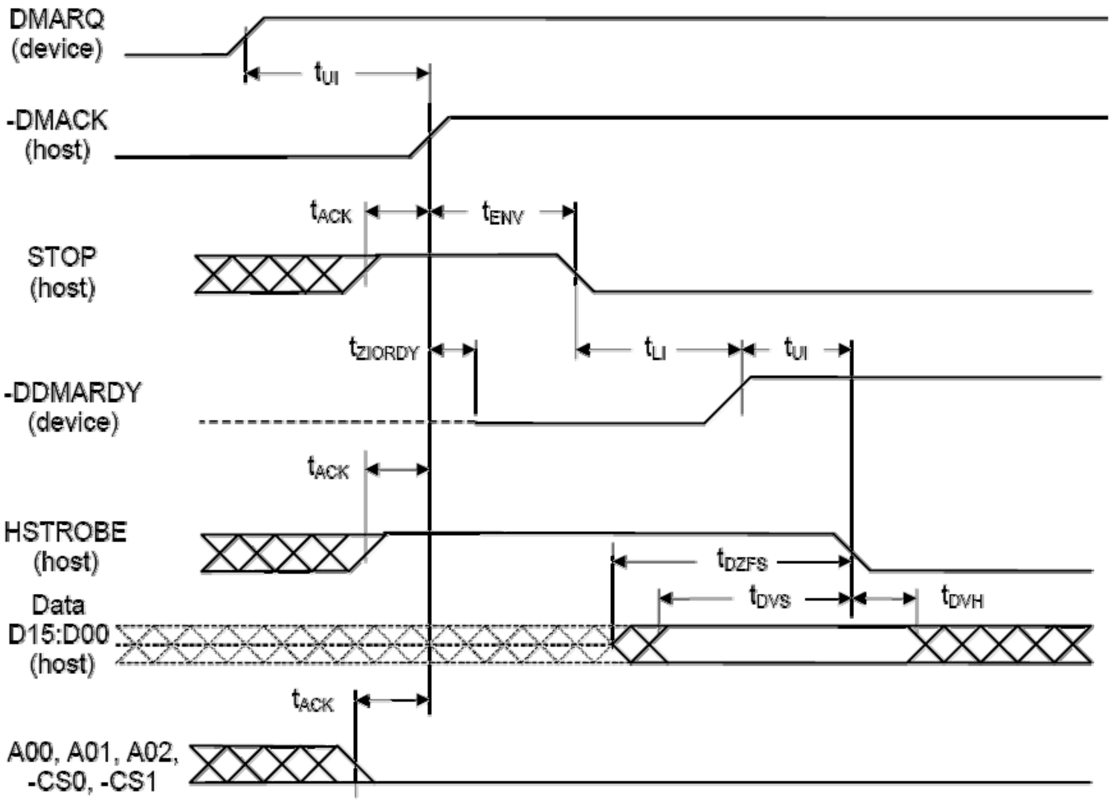
Notes:

The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

Initiating an Ultra DMA Data-Out Burst

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a. The host shall keep -DMACK in the negated state before an Ultra DMA burst is initiated.
b. The device shall assert DMARQ to initiate an Ultra DMA burst.
c. Steps (c), (d), and (e) may occur in any order or at the same time. The host shall assert STOP.
d. The host shall assert HSTROBE.
e. The host shall negate -CS0, -CS1, DA2, DA1, and DA0. The host shall keep -CS0, -CS1, DA2, DA1, and DA0 negated until after negating -DMACK at the end of the burst.
f. Steps (c), (d), and (e) shall have occurred at least tACK before the host asserts -DMACK. The host shall keep -DMACK asserted until the end of an Ultra DMA burst.
g. The device may negate -DDMARDY tZIORDY after the host has asserted -DMACK. Once the device has negated -DDMARDY, the device shall not release -DDMARDY until after the host has negated DMACK at the end of an Ultra DMA burst.
h. The host shall negate STOP within tENV after asserting -DMACK. The host shall not assert STOP until after the first negation of HSTROBE.
i. The device shall assert -DDMARDY within tLI after the host has negated STOP. After asserting DMARQ and -DDMARDY the device shall not negate either signal until after the first negation of HSTROBE by the host.
j. The host shall drive the first word of the data transfer onto D[15:00]. This step may occur any time during Ultra DMA burst initiation.
k. To transfer the first word of data: the host shall negate HSTROBE no sooner than tUI after the device has asserted -DDMARDY. The host shall negate HSTROBE no sooner than tDVS after the driving the first word of data onto D[15:00].



Note:

The definitions for the STOP, DDMARDY, and HSTROBE signal lines are not in effect until DMARQ and DMACK are asserted.

Sustaining an Ultra DMA Data-Out Burst

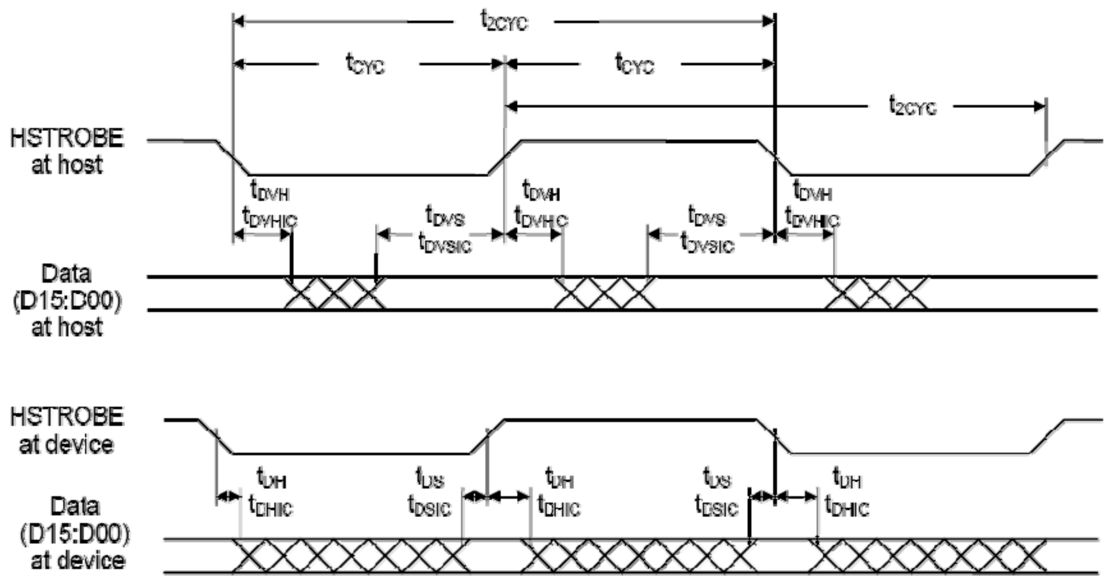
The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a. The host shall drive a data word onto D[15:00].

b. The host shall generate an HSTROBE edge to latch the new word no sooner than tDVS after changing the state of D[15:00]. The host shall generate an HSTROBE edge no more frequently than tCYC for the selected Ultra DMA mode. The host shall not generate two rising or falling HSTROBE edges more frequently than 2tcyc for the selected Ultra DMA mode.

c. The host shall not change the state of D[15:00] until at least tDVH after generating an HSTROBE edge to latch the data.

d. The host shall repeat steps (a), (b), and (c) until the data transfer is complete or an Ultra DMA burst is paused, whichever occurs first.



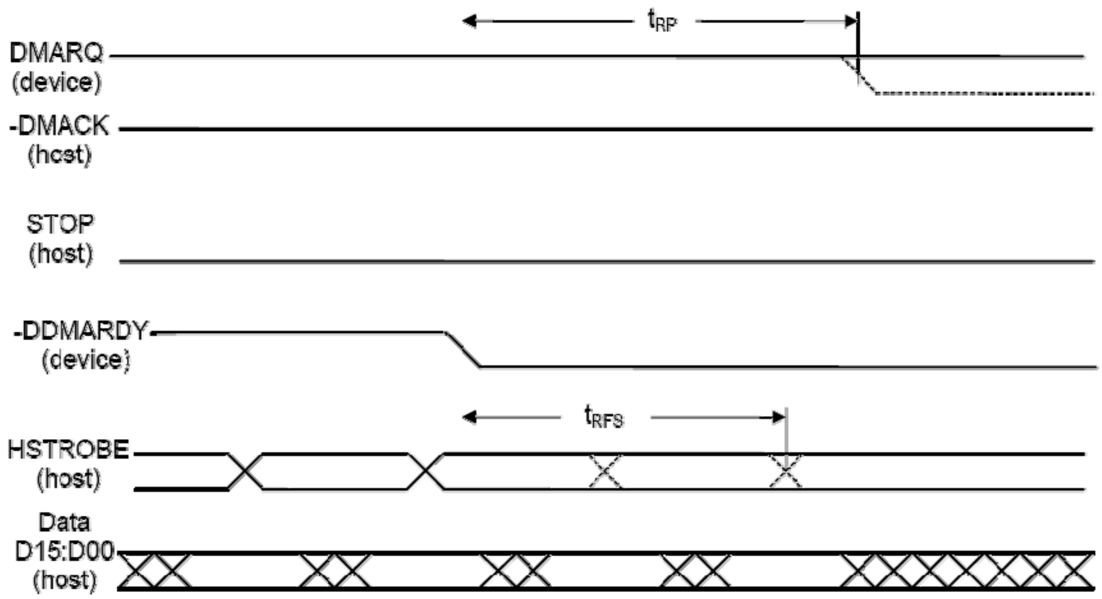
Note:

Data (D15:D00) and HSTROBE signals are shown at both the device and the host to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the device until some time after they are driven by the host.

Device Pausing an Ultra DMA Data-Out Burst

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a. The device shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.
b. The device shall pause an Ultra DMA burst by negating -DDMARDY.
c. The host shall stop generating HSTROBE edges within tRFS of the device negating -DDMARDY.
d. If the device negates -DDMARDY within tSR after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero or one additional data words. If the device negates -DDMARDY greater than tSR after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero, one or two additional data words. The additional data words are a result of cable round trip delay and tRFS timing for the host.
e. The device shall resume an Ultra DMA burst by asserting -DDMARDY.



Notes:

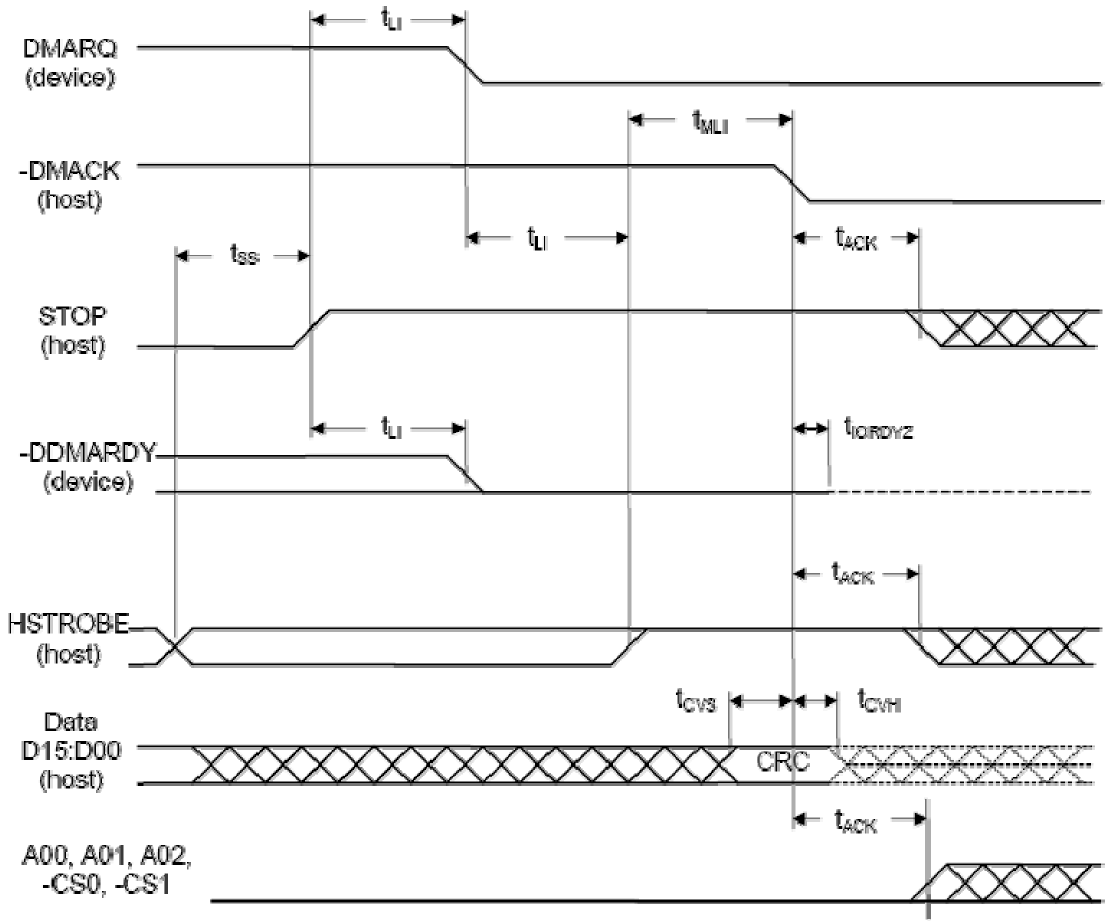
1) The device may negate DMARQ to request termination of the Ultra DMA burst no sooner than tRP after -DDMARDY is negated.

2) After negating -DDMARDY, the device may receive zero, one, two, or three more data words from the host.

Device Terminating an Ultra DMA Data-Out Burst

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a. The device shall not initiate Ultra DMA burst termination until at least one data word of an Ultra DMA burst has been transferred.
b. The device shall initiate Ultra DMA burst termination by negating -DDMARDY.
c. The host shall stop generating an HSTROBE edges within tRFS of the device negating -DDMARDY.
d. If the device negates -DDMARDY within tSR after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero or one additional data words. If the device negates -DDMARDY greater than tSR after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero, one or two additional data words. The additional data words are a result of cable round trip delay and tRFS timing for the host.
e. The device shall negate DMARQ no sooner than tRP after negating -DDMARDY. The device shall not assert DMARQ again until after the Ultra DMA burst is terminated.
f. The host shall assert STOP within tLI after the device has negated DMARQ. The host shall not negate STOP again until after the Ultra DMA burst is terminated.
g. If HSTROBE is negated, the host shall assert HSTROBE within tLI after the device has negated DMARQ. No data shall be transferred during this assertion. The device shall ignore this transition of HSTROBE. HSTROBE shall remain asserted until the Ultra DMA burst is terminated.
h. The host shall place the result of its CRC calculation on D[15:00].
i. The host shall negate -DMACK no sooner than tMLI after the host has asserted HSTROBE and STOP and the device has negated DMARQ and -DDMARDY, and no sooner than tDVS after placing the result of its CRC calculation on D[15:00].
j. The device shall latch the host's CRC data from D[15:00] on the negating edge of -DMACK.
k. The device shall compare the CRC data received from the host with the results of its own CRC calculation. If a miscompare error occurs during one or more Ultra DMA bursts for any one command.



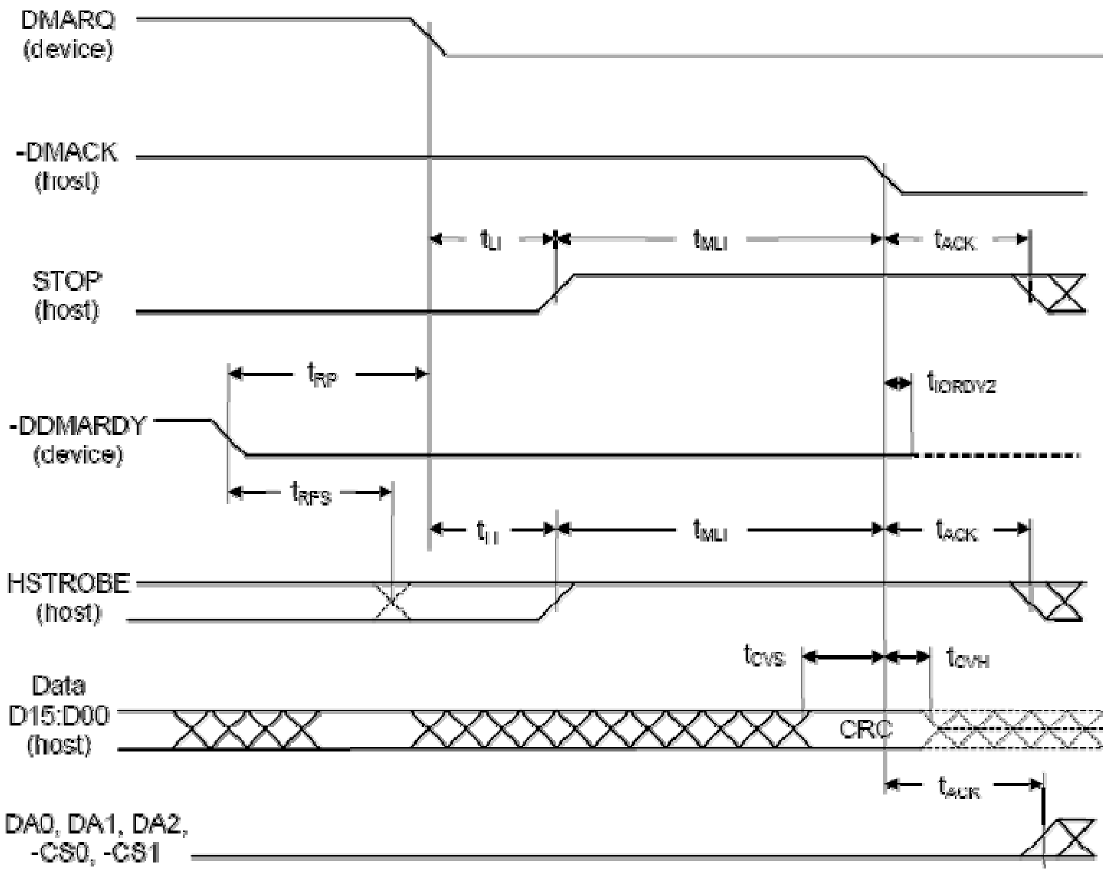
Note:

The definitions for the STOP, DDMARDY, and HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

Host Terminating an Ultra DMA Data-Out Burst

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a. The host shall initiate termination of an Ultra DMA burst by not generating HSTROBE edges.
b. The host shall assert STOP no sooner than tSS after it last generated an HSTROBE edge. The host shall not negate STOP again until after the Ultra DMA burst is terminated.
c. The device shall negate DMARQ within tLI after the host asserts STOP. The device shall not assert DMARQ again until after the Ultra DMA burst is terminated.
d. The device shall negate -DDMARDY within tLI after the host has negated STOP. The device shall not assert -DDMARDY again until after the Ultra DMA burst termination is complete.
e. If HSTROBE is negated, the host shall assert HSTROBE within tLI after the device has negated DMARQ. No data shall be transferred during this assertion. The device shall ignore this transition on HSTROBE. HSTROBE shall remain asserted until the Ultra DMA burst is terminated.
f. The host shall place the result of its CRC calculation on D[15:00] (see 9.15).
g. The host shall negate -DMACK no sooner than tMLI after the host has asserted HSTROBE and STOP and the device has negated DMARQ and -DDMARDY, and no sooner than tDVS after placing the result of its CRC calculation on D[15:00].
h. The device shall latch the host's CRC data from D[15:00] on the negating edge of -DMACK.
i. The device shall compare the CRC data received from the host with the results of its own CRC calculation. If a miscompare error occurs during one or more Ultra DMA bursts for any one command, at the end of the command, the device shall report the first error that occurred (see 9.15).
j. The device shall release -DDMARDY within t IORDYZ after the host has negated -DMACK.
k. The host shall neither negate STOP nor negate HSTROBE until at least tACK after negating -DMACK.
l. The host shall not assert -IOWR, -CS0, -CS1, DA2, DA1, or DA0 until at least tACK after negating -DMACK.



Notes:

The definitions for the STOP, DDMARDY, and HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

7) Ultra DMA CRC Calculation

The following is a list of rules for calculating CRC, determining if a CRC error has occurred during an Ultra DMA burst, and reporting any error that occurs at the end of a command.

a. Both the host and the device shall have a 16-bit CRC calculation function.
b. Both the host and the device shall calculate a CRC value for each Ultra DMA burst.
c. The CRC function in the host and the device shall be initialized with a seed of 4ABAh at the beginning of an Ultra DMA burst before any data is transferred.
d. For each STROBE transition used for data transfer, both the host and the device shall calculate a new CRC value by applying the CRC polynomial to the current value of their individual CRC functions and the word being transferred. CRC is not calculated for the return of STROBE to the asserted state after the Ultra DMA burst termination request has been acknowledged.
e. At the end of any Ultra DMA burst the host shall send the results of its CRC calculation function to the device on D[15:00] with the negation of -DMACK.
f. The device shall then compare the CRC data from the host with the calculated value in its own CRC calculation function. If the two values do not match, the device shall save the error and report it at the end of the command. A subsequent Ultra DMA burst for the same command that does not have a CRC error shall not clear an error saved from a previous Ultra DMA burst in the same command. If a miscompare error occurs during one or more Ultra DMA bursts for any one command, at the end of the command, the device shall report the first error that occurred.
g. For READ DMA, WRITE DMA, READ DMA QUEUED, or WRITE DMA QUEUED commands: When a CRC error is detected, it shall be reported by setting both ICRC and ABRT (bit 7 and bit 2 in the Error register) to one. ICRC is defined as the “Interface CRC Error” bit. The host shall respond to this error by re-issuing the command.
h. For a REQUEST SENSE packet command (see SPC T10/955D for definition of the REQUEST SENSE command): When a CRC error is detected during transmission of sense data the device shall complete the command and set CHK to one. The device shall report a Sense key of 0Bh (ABORTED COMMAND). The device shall preserve the original sense data that was being returned when the CRC error occurred. The device shall not report any additional sense data specific to the CRC error. The host device driver may retry the REQUEST SENSE command or may consider this an unrecoverable error and retry the command that caused the Check Condition.
i. For any packet command except a REQUEST SENSE command: If a CRC error is detected, the device shall complete the command with CHK set to one. The device shall report a Sense key of 04h (HARDWARE ERROR). The sense data supplied via a subsequent REQUEST SENSE command shall report an ASC/ASCQ value of 08h/03h

(LOGICAL UNIT COMMUNICATION CRC ERROR). Host drivers should retry the command that resulted in a HARDWARE ERROR.

NOTE

If excessive CRC errors are encountered while operating in Ultra mode 2 or 1, the host should select a slower Ultra mode. Caution: CRC errors are detected and reported only while operating in an Ultra mode.

j. A host may send extra data words on the last Ultra DMA burst of a data out command. If a device determines that all data has been transferred for a command, the device shall terminate the burst. A device may have already received more data words than were required for the command. These extra words are used by both the host and the device to calculate the CRC, but, on an Ultra DMA data out burst, the extra words shall be discarded by the device.

k. The CRC generator polynomial is: G(X) = X16 + X12 + X5 + 1. Table 28 describes the equations for 16-bit parallel generation of the resulting polynomial (based on a word boundary).

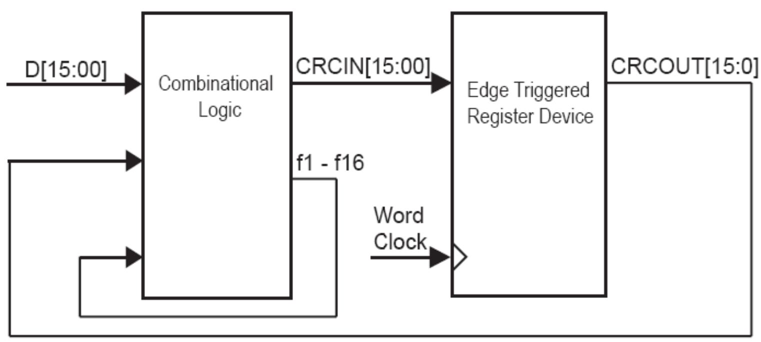
NOTE

Since no bit clock is available, the recommended approach for calculating CRC is to use a word clock derived from the bus strobe. The combinational logic is then equivalent to shifting sixteen bits serially through the generator polynomial where D00 is shifted in first and D15 is shifted in last.

CRCIN0 = f16	CRCIN8 = f8 XOR f13
CRCIN1 = f15	CRCIN9 = f7 XOR f12
CRCIN2 = f14	CRCIN10 = f6 XOR f11
CRCIN3 = f13	CRCIN11 = f5 XOR f10
CRCIN4 = f12	CRCIN12 = f4 XOR f9 XOR f16
CRCIN5 = f11 XOR f16	CRCIN13 = f3 XOR f8 XOR f15
CRCIN6 = f10 XOR f15	CRCIN14 = f2 XOR f7 XOR f14
CRCIN7 = f9 XOR f14	CRCIN15 = f1 XOR f6 XOR f13
f1 = D00 XOR CRCOUT15	f9 = D08 XOR CRCOUT7 XOR f5
f2 = D01 XOR CRCOUT14	f10 = D09 XOR CRCOUT6 XOR f6
f3 = D02 XOR CRCOUT13	f11 = D10 XOR CRCOUT5 XOR f7
f4 = D03 XOR CRCOUT12	f12 = D11 XOR CRCOUT4 XOR f1 XOR f8
f5 = D04 XOR CRCOUT11 XOR f1	f13 = D12 XOR CRCOUT3 XOR f2 XOR f9
f6 = D05 XOR CRCOUT10 XOR f2	f14 = D13 XOR CRCOUT2 XOR f3 XOR f10
f7 = D06 XOR CRCOUT9 XOR f3	f15 = D14 XOR CRCOUT1 XOR f4 XOR f11
f8 = D07 XOR CRCOUT8 XOR f4	f16 = D15 XOR CRCOUT0 XOR f5 XOR f12

Notes:
1) f=feedback
2) D[15:0] = Data to or from the bus
3) CRCOUT = 16-bit edge triggered result (current CRC)
4) CRCOUT[15:0] are sent on matching order bits of D[15:00]

An example of a CRC generator implementation is provided below in Figure 43: Ultra DMA Parallel CRC Generator Example.



6.6. CompactFlash™ Card Registers and Memory Space Decoding

-CE2	-CE1	-REG	-OE	-WE	A10	A9	A8-A4	A3	A2	A1	A0	SELECTED SPACE
1	1	X	X	X	X	X	XX	X	X	X	X	Standby
X	0	0	0	1	0	1	XX	X	X	X	0	Configuration Registers Read
1	0	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8 Bit D7-D0)
0	1	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8 Bit D15-D8)
0	0	1	0	1	X	X	XX	X	X	X	0	Common Memory Read (16 Bit D15-D0)
X	0	0	1	0	0	1	XX	X	X	X	0	Configuration Registers Write
1	0	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8 Bit D7-D0)
0	1	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8 Bit D15-D8)
0	0	1	1	0	X	X	XX	X	X	X	0	Common Memory Write (16 Bit D15-D0)
X	0	0	0	1	0	0	XX	X	X	X	0	Card Information Structure Read
1	0	0	1	0	0	0	XX	X	X	X	0	Invalid Access (CIS Write)
1	0	0	0	1	X	X	XX	X	X	X	1	Invalid Access (Odd Attribute Read)
1	0	0	1	0	X	X	XX	X	X	X	1	Invalid Access (Odd Attribute Write)
0	1	0	0	1	X	X	XX	X	X	X	X	Invalid Access (Odd Attribute Read)
0	1	0	1	0	X	X	XX	X	X	X	X	Invalid Access (Odd Attribute Write)

6.6.1. Attribute Memory Function

Attribute memory is a space where CompactFlash™ Storage Card and CF+ Card identification and configuration information are stored, and is limited to 8 bit wide accesses only at even addresses. The card configuration registers are also located here. For CompactFlash™ Storage Cards, the base address of the card configuration registers is 200h. For CF+ cards, the base address of the card configuration registers is determined by the Configuration tuple (CISTPL_CONFIG). For the Attribute Memory Read function, signals -REG and -OE must be active and -WE inactive during the cycle. As in the Main Memory Read functions, the signals -CE1 and -CE2 control the even-byte and odd-byte address, but only the even-byte data is valid during the Attribute Memory access. Refer to Table 24: Attribute Memory Function below for signal states and bus validity for the Attribute Memory function.

Function Mode	-REG	-CE2	-CE1	A10	A9	A0	-OE	-WE	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	X	X	High Z	High Z
Read Byte Access CIS ROM (8 bits)	L	H	L	L	L	L	L	H	High Z	Even Byte
Write Byte Access CIS (8 bits) (Invalid)	L	H	L	L	L	L	H	L	Don't Care	Even Byte
Read Byte Access Configuration CompactFlash Storage (8 bits)	L	H	L	L	H	L	L	H	High Z	Even Byte
Write Byte Access Configuration CompactFlash Storage (8 bits)	L	H	L	L	H	L	H	L	Don't Care	Even Byte
Read Byte Access Configuration *CF+* (8 bits)	L	H	L	X	X	L	L	H	High Z	Even Byte
Write Byte Access Configuration *CF+* (8 bits)	L	H	L	X	X	L	H	L	Don't Care	Even Byte
Read Word Access CIS (16 bits)	L	L	L	L	L	X	L	H	Not Valid	Even Byte
Write Word Access CIS (16 bits) (Invalid)	L	L	L	L	L	X	H	L	Don't Care	Even Byte
Read Word Access Configuration CompactFlash Storage (16 bits)	L	L	L	L	H	X	L	H	Not Valid	Even Byte
Write Word Access Configuration CompactFlash Storage (16 bits)	L	L	L	L	H	X	H	L	Don't Care	Even Byte
Read Word Access Configuration *CF+* (16 bits)	L	L	L	X	X	X	L	H	Not Valid	Even Byte
Write Word Access Configuration *CF+* (16 bits)	L	L	L	X	X	X	H	L	Don't Care	Even Byte

6.6.2. I/O function

The I/O transfer to or from the CompactFlash™ Storage or CF+ Card can be either 8 or 16 bits. When a 16 bit accessible port is addressed, the signal -IOIS16 is asserted by the CompactFlash™ Storage or CF+ Card. Otherwise, the -IOIS16 signal is de-asserted. When a 16 bit transfer is attempted, and the -IOIS16 signal is not asserted by the CompactFlash™ Storage or CF+ Card, the system must generate a pair of 8 bit references to access the word's even byte and odd byte. The CompactFlash™ Storage Card permits both 8 and 16 bit accesses to all of its I/O addresses, so -IOIS16 is asserted for all addresses to which the CompactFlash™ Storage responds. CF+ cards may or may not allow 16 bit register accesses and thus must assert IOIS16 as required. The CompactFlash™ Storage and CF+ Card may request the host to extend the length of an input cycle until data is ready by asserting the -WAIT signal at the start of the cycle.

Function Code	-REG	-CE2	-CE1	A0	-IORD	-IOWR	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	High Z	High Z
Byte Input Access (8 bits)	L L	H H	L L	L H	L L	H H	High Z High Z	Even-Byte Odd-Byte
Byte Output Access (8 bits)	L L	H H	L L	L H	H H	L L	Don't Care Don't Care	Even-Byte Odd-Byte
Word Input Access (16 bits)	L	L	L	L	L	H	Odd-Byte	Even-Byte
Word Output Access (16 bits)	L	L	L	L	H	L	Odd-Byte	Even-Byte
I/O Read Inhibit	H	X	X	X	L	H	Don't Care	Don't Care
I/O Write Inhibit	H	X	X	X	H	L	High Z	High Z
High Byte Input Only (8 bits)	L	L	H	X	L	H	Odd-Byte	High Z
High Byte Output Only (8 bits)	L	L	H	X	H	L	Odd-Byte	Don't Care

6.6.3. Common Memory Function

The Common Memory transfer to or from the CompactFlash™ Storage or CF+ Card can be either 8 or 16 bits .The CompactFlash™ Storage Card and the CF+ Card permit both 8 and 16 bit accesses to all of its Common Memory addresses. The CompactFlash™ Storage Card or the CF+ Card may request the host to extend the length of a memory write cycle or extend the length of a memory read cycle until data is ready by asserting the -WAIT signal at the start of the cycle.

Function Code	-REG	-CE2	-CE1	A0	-OE	-WE	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	High Z	High Z
Byte Read Access (8 bits)	H H	H H	L L	L H	L L	H H	High Z High Z	Even-Byte Odd-Byte
Byte Write Access (8 bits)	H H	H H	L L	L H	H H	L L	Don't Care Don't Care	Even-Byte Odd-Byte
Word Read Access (16 bits)	H	L	L	X	L	H	Odd-Byte	Even-Byte
Word Write Access (16 bits)	H	L	L	X	H	L	Odd-Byte	Even-Byte
Odd Byte Read Only (8 bits)	H	L	H	X	L	H	Odd-Byte	High Z
Odd Byte Write Only (8 bits)	H	L	H	X	H	L	Odd-Byte	Don't Care

6.6.4. True IDE Mode I/O Function

The CompactFlash™ Storage Card and CF+ Card can be configured in a True IDE Mode of operation. The CompactFlash™ Storage Card is configured in this mode only when the -OE input signal is grounded by the host during the power off to power on cycle. Optionally, CompactFlash™ Storage Cards and CF+ Cards may support the following optional detection methods:

1. The card is permitted to monitor the –OE (-ATA SEL) signal at any time(s) and switch to PCMCIA mode upon detecting a high level on the pin.

2. The card is permitted to re-arbitrate the interface mode determination following a transition of the (-)RESET pin.

3. The card is permitted to monitor the –OE (-ATA SEL) signal at any time(s) and switch to True IDE mode upon detection of a continuous low level on pin for an extended period of time. Host implementers should not rely on any of these optional detection methods in their designs. In the True IDE Mode, the PCMCIA protocol and configuration are disabled and only I/O operations to the Task File and Data Register are allowed. In this mode, no Memory or Attribute Registers are accessible to the host. CompactFlash™ Storage Cards permit 8 bit data accesses if the user issues a Set Feature Command to put the CompactFlash™ Storage Card in 8 bit Mode.

Function Code	-CS1	-CS0	A0-A2	-DMACK	-IORD	-IOWR	D15-D8	D7-D0
Invalid Modes	L	L	X	X	X	X	Undefined In/Out	Undefined In/Out
	L	X	X	L	L	X	Undefined Out	Undefined Out
	L	X	X	L	X	L	Undefined In	Undefined In
	X	L	X	L	L	X	Undefined Out	Undefined Out
	X	L	X	L	X	L	Undefined In	Undefined In
Standby Mode	H	H	X	H	X	X	High Z	High Z
Task File Write	H	L	1-7h	H	H	L	Don't Care	Data In
Task File Read	H	L	1-7h	H	L	H	High Z	Data Out
PIO Data Register Write	H	L	0	H	H	L	Odd-Byte In	Even-Byte In
DMA Data Register Write	H	H	X	L	H	L	Odd-Byte In	Even-Byte In
Ultra DMA Data Register Write	H	H	X	L	See Note 2		Odd-Byte In	Even-Byte In
PIO Data Register Read	H	L	0	H	L	H	Odd-Byte Out	Even-Byte Out
DMA Data Register Read	H	H	X	L	L	H	Odd-Byte Out	Even-Byte Out
Ultra DMA Data Register Read	H	H	X	L	See Note 3		Odd-Byte Out	Even-Byte Out
Control Register Write	L	H	6h	H	H	L	Don't Care	Control In
Alt Status Read	L	H	6h	H	L	H	High Z	Status Out
Drive Address[1]	L	H	7h	H	L	H	High Z	Data Out

6.7. I/O Primary and Secondary Address Configurations

6.7.1. Primary and Secondary I/O Decoding

-REG	A9-A4	A3	A2	A1	A0	-IORD=0	-IOWR=0
0	1F(17)h	0	0	0	0	Even RD Data	Even WR Data
0	1F(17)h	0	0	0	1	Error Register	Features
0	1F(17)h	0	0	1	0	Sector Count	Sector Count
0	1F(17)h	0	0	1	1	Sector No.	Sector No.
0	1F(17)h	0	1	0	0	Cylinder Low	Cylinder Low
0	1F(17)h	0	1	0	1	Cylinder High	Cylinder High
0	1F(17)h	0	1	1	0	Select Card/Head	Select Card/Head
0	1F(17)h	0	1	1	1	Status	Command
0	3F(37)h	0	1	1	0	Alt Status	Device Control
0	3F(37)h	0	1	1	1	Drive Address	Reserved

6.7.2. Contiguous I/O Mapped Addressing & Decoding

When the system decodes a contiguous block of I/O registers to select the CompactFlash™ Storage Card, the registers are accessed in the block of I/O space decoded by the system as follows:

-REG	A3	A2	A1	A0	Offset	-IORD=0	-IOWR=0
0	0	0	0	0	0	Even RD Data	Even WR Data
0	0	0	0	1	1	Error	Features
0	0	0	1	0	2	Sector Count	Sector Count
0	0	0	1	1	3	Sector No.	Sector No.
0	0	1	0	0	4	Cylinder Low	Cylinder Low
0	0	1	0	1	5	Cylinder High	Cylinder High
0	0	1	1	0	6	Select Card /Head	Select Card/Head
0	0	1	1	1	7	Status	Command
0	1	0	0	0	8	Dup Even RD Data	Dup. Even WR Data
0	1	0	0	1	9	Dup. Odd RD Data	Dup. Odd WR Data
0	1	1	0	1	D	Dup. Error	Dup. Features
0	1	1	1	0	E	Alt Status	Device Ctl
0	1	1	1	1	F	Drive Address	Reserved

6.7.3. *Memory Mapped Addressing & Decoding*

When the CompactFlash™ Storage Card registers are accessed via memory references, the registers appear in the common memory space window: 0-2K bytes as follows:

-REG	A10	A9-A4	A3	A2	A1	A0	Offset	-OE=0	-WE=0
1	0	X	0	0	0	0	0	Even RD Data	Even WR Data
1	0	X	0	0	0	1	1	Error	Features
1	0	X	0	0	1	0	2	Sector Count	Sector Count
1	0	X	0	0	1	1	3	Sector No.	Sector No.
1	0	X	0	1	0	0	4	Cylinder Low	Cylinder Low
1	0	X	0	1	0	1	5	Cylinder High	Cylinder High
1	0	X	0	1	1	0	6	Select Card /Head	Select Card/Head
1	0	X	0	1	1	1	7	Status	Command
1	0	X	1	0	0	0	8	Dup. Even RD Data	Dup. Even WR Data
1	0	X	1	0	0	1	9	Dup. Odd RD Data	Dup. Odd WR Data
1	0	X	1	1	0	1	D	Dup. Error	Dup. Features
1	0	X	1	1	1	0	E	Alt Status	Device Ctl
1	0	X	1	1	1	1	F	Drive Address	Reserved
1	1	X	X	X	X	0	8	Even RD Data	Even WR Data
1	1	X	X	X	X	1	9	Odd RD Data	Odd WR Data

6.7.4. *True IDE Mode Addressing*

When the CompactFlash™ Storage Card is configured in the True IDE Mode, the I/O decoding is as follows:

-CS1	-CS0	A2	A1	A0	-DMACK	-IORD=0	-IOWR=0	Note
1	0	0	0	0	1	PIO RD Data	PIO WR Data	8 or 16 bit[1]
1	1	X	X	X	0	DMA RD Data	DMA WR Data	16 bit
1	0	0	0	1	1	Error Register	Features	8 bit
1	0	0	1	0	1	Sector Count	Sector Count	8 bit
1	0	0	1	1	1	Sector No.	Sector No.	8 bit
1	0	1	0	0	1	Cylinder Low	Cylinder Low	8 bit
1	0	1	0	1	1	Cylinder High	Cylinder High	8 bit
1	0	1	1	0	1	Select Card/Head	Select Card/Head	8 bit
1	0	1	1	1	1	Status	Command	8 bit
0	1	1	1	0	1	Alt Status	Device Control	8 bit

6.8. Power Management

CompactFlash™ Card provides automatic power saving mode.

There are three modes on this system:

1. Standby Mode: When the CompactFlash™ finished initialization after power reset or hardware reset, it goes into Standby Mode to wait for Command In or Soft Reset.

2. Active Mode: If the CompactFlash™ received any Command In or Soft Reset, it goes into Active Mode. In Active Mode, it is capable of executing any ATA commands. The power consumption is the greatest in this mode.

3. Sleep Mode: The CompactFlash™ will enter Sleep Mode if there is no Command In or Soft Reset from the host for about 4ms or sleep command is asserted. This time interval can be modified by firmware if necessary. Sleep Mode provides the lowest power consumption. During Sleep Mode, the system main clock is stopped. This mode can be waked up from hardware reset, software reset or any ATA command asserted.

7. CF – ATA Command Description

This section defines the software requirements and the format of the commands the host sends to the CompactFlash™ Storage Cards. Commands are issued to the CompactFlash™ Storage Card by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command Register. The manner in which a command is accepted varies. There are three classes (see Table 37: CF-ATA Command Set) of command acceptance, all dependent on the host not issuing commands unless the CompactFlash™ Storage Card is not busy (BSY=0). All commands listed in this specification shall be implemented. Commands can be implemented as "no operation" to meet this requirement. The Security Mode feature set (command codes F1, F2, F3, F4, F5, and F6) should not be implemented unless the device is intended to be used in an embedded, non-removable application. The Security Mode feature set was not designed for removable devices and certain problems may be encountered when using these commands in a removable application. This specification introduces some new commands and features. If these commands are used on an older CF card, an Invalid Command Error may occur. Upon receipt of a Class 1 command, the CompactFlash™ Storage Card sets BSY within 400 nsec. Upon receipt of a Class 2 command, the CompactFlash™ Storage Card sets BSY within 400 nsec, sets up the sector buffer for a write operation, sets DRQ within 700 µsec, and clears

BSY within 400 nsec of setting DRQ. Upon receipt of a Class 3 command, the CompactFlash™ Storage Card sets BSY within 400 nsec, sets up the sector buffer for a write operation, sets DRQ within 20 msec (assuming no re-assignments), and clears BSY within 400 nsec of setting DRQ.

7.1. CF – ATA Command Set

CF-ATA Command Set summarizes the CF-ATA command set with the paragraphs that follow describing the individual commands and the task file for each.

Class	COMMAND	Code	FR	SC	SN	CY	DH	LBA
1	Check Power Mode	E5h or 98h	-	-	-	-	D	-
1	Execute Drive Diagnostic	90h	-	-	-	-	D	-
1	Erase Sector(s)	C0h	-	Y	Y	Y	Y	Y
1	Flush Cache	E7h	-	-	-	-	D	-
2	Format Track	50h	-	Y	-	Y	Y	Y
1	Identify Device	ECh	-	-	-	-	D	-
1	Idle	E3h or 97h	-	Y	-	-	D	-
1	Idle Immediate	E1h or 95h	-	-	-	-	D	-
1	Initialize Drive Parameters	91h	-	Y	-	-	Y	-
1	Key Management Structure Read	B9 Feature 0-127	C	C	C	C	D C	-
1	Key Management Read Keying Material	B9 Feature 80	C	C	C	C	D C	-
2	Key Management Change Key Management Value	B9 Feature 81	C	C	C	C	D C	-
1	NOP	00h	-	-	-	-	D	-
1	Read Buffer	E4h	-	-	-	-	D	-
1	Read DMA	C8h	-	Y	Y	Y	Y	Y
1	Read Long Sector	22h or 23h	-	-	Y	Y	Y	Y
1	Read Multiple	C4h	-	Y	Y	Y	Y	Y
1	Read Sector(s)	20h or 21h	-	Y	Y	Y	Y	Y
1	Read Verify Sector(s)	40h or 41h	-	Y	Y	Y	Y	Y
1	Recalibrate	1Xh	-	-	-	-	D	-
1	Request Sense	03h	-	-	-	-	D	-
1	Security Disable Password	F6h	-	-	-	-	D	-
1	Security Erase Prepare	F3h	-	-	-	-	D	-
1	Security Erase Unit	F4h	-	-	-	-	D	-
1	Security Freeze Lock	F5h	-	-	-	-	D	-
1	Security Set Password	F1h	-	-	-	-	D	-
1	Security Unlock	F2h	-	-	-	-	D	-
1	Seek	7Xh	-	-	Y	Y	Y	Y
1	Set Features	EFh	Y	-	-	-	D	-
1	Set Multiple Mode	C6h	-	Y	-	-	D	-

Class	COMMAND	Code	FR	SC	SN	CY	DH	LBA
1	Set Sleep Mode	E6h or 99h	-	-	-	-	D	-
1	Standby	E2h or 96h	-	-	-	-	D	-
1	Standby Immediate	E0h or 94h	-	-	-	-	D	-
1	Translate Sector	87h	-	Y	Y	Y	Y	Y
1	Wear Level	F5h	-	-	-	-	Y	-
2	Write Buffer	E8h	-	-	-	-	D	-
2	Write DMA	CAh	-	Y	Y	Y	Y	Y
2	Write Long Sector	32h or 33h	-	-	Y	Y	Y	Y
3	Write Multiple	C5h	-	Y	Y	Y	Y	Y
3	Write Multiple w/o Erase	CDh	-	Y	Y	Y	Y	Y
2	Write Sector(s)	30h or 31h	-	Y	Y	Y	Y	Y
2	Write Sector(s) w/o Erase	38h	-	Y	Y	Y	Y	Y
3	Write Verify	3Ch	-	Y	Y	Y	Y	Y

Definitions:

FR = Features Register

SC = Sector Count R egister

SN = Sector Number Register

CY = Cylinder Registers

DH = Card/Drive/Head Register

LBA = Logical Block

Address Mode Supported (see command descriptions for use). Y - The register contains a valid parameter for this command. For the Drive/Head Register Y means both the CompactFlash™ Storage Card and head parameters are used; D - only the CompactFlash™ Storage Card parameter is valid and not the head parameter; C – The register contains command specific data (see command descriptions for use).

7.1.1. Identify Drive – Ech

Bit ->	7	6	5	4	3	2	1	0
Command (7)	ECh							
C/D/H (6)	X	X	X	Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

The Identify Drive command enables the host to receive parameter information from the CompactFlash™ Storage Card. This command has the same protocol as the Read Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in Table 39. All reserved bits or words are zero. Hosts should not depend on Obsolete words in Identify Drive containing 0. Table 39 specifies each field in the data returned by the Identify Drive Command. In Table 39, X indicates a numeric nibble value specific to the card and aaaa indicates an ASCII string specific to the particular drive.

7.1.2. Identify Drive Information

Word Address	Default Value	Total Bytes	Data Field Type Information
0	848Ah	2	General configuration - signature for the CompactFlash Storage Card
	0XXX	2	General configuration – Bit Significant with ATA-4 definitions.
1	XXXXh	2	Default number of cylinders
2	0000h	2	Reserved
3	00XXh	2	Default number of heads
4	0000h	2	Obsolete
5	0000h	2	Obsolete
6	XXXXh	2	Default number of sectors per track
7-8	XXXXh	4	Number of sectors per card (Word 7 = MSW, Word 8 = LSW)
9	XXXXh	2	Obsolete
10-19	aaaa	20	Serial number in ASCII (Right Justified)
20	0000h	2	Obsolete
21	0000h	2	Obsolete
22	0004h	2	Number of ECC bytes passed on Read/Write Long Commands
23-26	aaaa	8	Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	aaaa	40	Model number in ASCII (Left Justified) Big Endian Byte Order in Word
47	XXXXh	2	Maximum number of sectors on Read/Write Multiple command
48	0000h	2	Reserved

Word Address	Default Value	Total Bytes	Data Field Type Information
49	XX00h	2	Capabilities
50	0000h	2	Reserved
51	0X00h	2	PIO data transfer cycle timing mode
52	0000h	2	Obsolete
53	000Xh	2	Field Validity
54	XXXXh	2	Current numbers of cylinders
55	XXXXh	2	Current numbers of heads
56	XXXXh	2	Current sectors per track
57-58	XXXXh	4	Current capacity in sectors (LBAs)(Word 57 = LSW, Word 58 = MSW)
59	01XXh	2	Multiple sector setting
60-61	XXXXh	4	Total number of sectors addressable in LBA Mode
62	0000h	2	Reserved
63	0X0Xh	2	Multiword DMA transfer. In PCMCIA mode this value shall be 0h
64	00XXh	2	Advanced PIO modes supported
65	XXXXh	2	Minimum Multiword DMA transfer cycle time per word. In PCMCIA mode this value shall be 0h
66	XXXXh	2	Recommended Multiword DMA transfer cycle time. In PCMCIA mode this value shall be 0h
67	XXXXh	2	Minimum PIO transfer cycle time without flow control
68	XXXXh	2	Minimum PIO transfer cycle time with IORDY flow control
69-79	0000h	20	Reserved
80-81	0000h	4	Reserved – CF cards do not return an ATA version
82-84	XXXXh	6	Features/command sets supported
85-87	XXXXh	6	Features/command sets enabled
88	XXXXh	2	Ultra DMA Mode Supported and Selected
89	XXXXh	2	Time required for Security erase unit completion
90	XXXXh	2	Time required for Enhanced security erase unit completion
91	XXXXh	2	Current Advanced power management value
92-127	0000h	72	Reserved
128	XXXXh	2	Security status
129-159	0000h	64	Vendor unique bytes
160	XXXXh	2	Power requirement description
161	0000h	2	Reserved for assignment by the CFA
162	0000h	2	Key management schemes supported
163	XXXXh	2	CF Advanced True IDE Timing Mode Capability and Setting
164	XXXXh	2	CF Advanced PCMCIA I/O and Memory Timing Mode Capability
165-175	0000h	22	Reserved for assignment by the CFA

Word Address	Default Value	Total Bytes	Data Field Type Information
176-255	0000h	140	Reserved

Word 0: General Configuration

This field indicates that the device is a CompactFlash™ Storage Card. Note to host implementers: If Word 0 of the Identify drive information is 848Ah then the device complies with the CFA specification, not with the ATA-4 specification.

Word 1: Default Number of Cylinders

This field contains the number of translated cylinders in the default translation mode. This value will be the same as the number of cylinders.

Word 3: Default Number of Heads

This field contains the number of translated heads in the default translation mode.

Word 6: Default Number of Sectors per Track

This field contains the number of sectors per track in the default translation mode.

Words 7-8: Number of Sectors per Card

This field contains the number of sectors per CompactFlash™ Storage Card. This double word value is also the first invalid address in LBA translation mode.

Words 10-19: Serial Number

This field contains the serial number for this CompactFlash™ Storage Card and is right justified and padded with spaces (20h).

Word 22: ECC Count

This field defines the number of ECC bytes used on each sector in the Read and Write Long commands. This value shall be set to 0004h.

Words 23-26: Firmware Revision

This field contains the revision of the firmware for this product.

Words 27-46: Model Number

This field contains the model number for this product and is left justified and padded with spaces (20h).

Word 47: Read/Write Multiple Sector Count

Bits 15-8 shall be the recommended value of 80h or the permitted value of 00h. Bits 7-0 of this word define the maximum number of sectors per block that the CompactFlash™ Storage Card supports for Read/Write Multiple commands.

Word 49: Capabilities

Bit 13: Standby Timer If bit 13 is set to 1 then the Standby timer is supported as defined by the IDLE command If bit 13 is set to 0 then the Standby timer operation is defined by the vendor. Bit 11: IORDY Supported If bit 11 is set to 1 then this CompactFlash™ Storage Card supports IORDY operation. If bit 11 is set to 0 then this CompactFlash™ Storage Card may support IORDY operation. Bit 10: IORDY may be disabled Bit 10 shall be set to 0, indicating that IORDY may not be disabled. Bit 9: LBA supported Bit 9 shall be set to 1, indicating that this CompactFlash™ Storage Card supports LBA mode addressing. CF devices shall support LBA addressing. Bit 8: DMA Supported If bit 8 is set to 1 then Read DMA and Write DMA commands are supported. Bit 8 shall be set to 0. Read/Write DMA commands are not currently permitted on CF cards.

Word 51: PIO Data Transfer Cycle Timing Mode

The PIO transfer timing for each CompactFlash™ Storage Card falls into modes that have unique parametric timing specifications. The value returned in Bits 15-8 shall be 00h for mode 0, 01h for mode 1, or 02h for mode 2. Values 03h through FFh are reserved.

Word 53: Translation Parameters Valid

Bit 0 shall be set to 1 indicating that words 54 to 58 are valid and reflect the current number of cylinders, heads and sectors. If bit 1 of word 53 is set to 1, the values in words 64 through 70 are valid. If this bit is cleared to 0, the values reported in words 64-70 are not valid. Any CompactFlash™ Storage Card that supports PIO mode 3 or above shall set bit 1 of word 53 to one and support the fields contained in words 64 through 70.

Words 54-56: Current Number of Cylinders, Heads, Sectors/Track

These fields contain the current number of user addressable Cylinders, Heads, and Sectors/Track in the current translation mode.

Words 57-58: Current Capacity

This field contains the product of the current cylinders times heads times sectors.

Word 59: Multiple Sector Setting

Bits 15-9 are reserved and shall be set to 0. Bit 8 shall be set to 1 indicating that the Multiple Sector Setting is valid. Bits 7-0 are the current setting for the number of sectors that shall be transferred per interrupt on Read/Write Multiple commands.

Words 60-61: Total Sectors Addressable in LBA Mode

This field contains the total number of user addressable sectors for the CompactFlash™ Storage Card in LBA mode only.

Word 64: Advanced PIO transfer modes supported

Bits 7 through 0 of word 64 of the Identify Device parameter information is defined as the advanced PIO data transfer supported field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant. Any number of bits may be set to one in this field by the CompactFlash™ Storage Card to indicate the advanced PIO modes it is capable of supporting. Of these bits, bits 7 through 2 are reserved for future advanced PIO modes. Bit 0, if set to one, indicates that the CompactFlash™ Storage Card supports PIO mode 3. Bit 1, if set to one, indicates that the CompactFlash™ Storage Card supports PIO mode 4.

Word 67: Minimum PIO transfer cycle time without flow control

Word 67 of the parameter information of the Identify Device command is defined as the minimum PIO transfer without flow control cycle time. This field defines, in nanoseconds, the minimum cycle time that, if used by the host, the CompactFlash™ Storage Card guarantees data integrity during the transfer without utilization of flow control. If this field is supported, Bit 1 of word 53 shall be set to one. Any CompactFlash™ Storage Card that supports PIO mode 3 or above shall support this field, and the value in word 67 shall not be less than the value reported in word 68. If bit 1 of word 53 is set to one because a CompactFlash™ Storage Card supports a field in words 64-70 other than this field and the CompactFlash™ Storage Card does not support this field, the CompactFlash™ Storage Card shall return a value of zero in this field.

Word 68: Minimum PIO transfer cycle time with IORDY

Word 68 of the parameter information of the Identify Device command is defined as the minimum PIO transfer with IORDY flow control cycle time. This field defines, in nanoseconds, the minimum cycle time that the CompactFlash™ Storage Card supports while performing data transfers while utilizing IORDY flow control. If this field is supported, Bit 1 of word 53 shall be set to one. Any CompactFlash™ Storage Card that supports PIO mode 3 or above shall support this field, and the value in word 68 shall be the fastest defined PIO mode supported by the CompactFlash™ Storage Card. If bit 1 of word 53 is set to one because a CompactFlash™ Storage Card supports a field in words 64-70 other than this field and the CompactFlash™ Storage Card does not support this field, the CompactFlash™ Storage Card shall return a value of zero in this field.

Words 82-84: Features/command sets supported

Words 82, 83, and 84 shall indicate features/command sets supported. The value 0000h or FFFFh was placed in each of these words by CompactFlash™ Storage Cards prior to ATA-3 and shall be interpreted by the host as meaning that features/command sets supported are not indicated. Bits 1 through 13 of word 83 and bits 0 through 13 of word 84 are reserved. Bit 14 of word 83 and word 84 shall be set to one and bit 15 of word 83 and word 84 shall be cleared to zero to provide indication that the features/command sets supported words are valid. The values in these words should not be depended on by host implementers. Bit 0 of word 82 shall be set to zero; the SMART feature set is not supported. If bit 1 of word 82 is set to one, the Security Mode feature set is supported. Bit 2 of word 82 shall be set to zero; the Removable Media feature set is not supported. Bit 3 of word 82 shall be set to one; the Power Management feature set is supported. Bit 4 of word 82 shall be set to zero; the Packet Command feature set is not supported. If bit 5 of word 82 is set to one, write cache is supported. If bit 6 of word 82 is set to one, look-ahead is supported. Bit 7 of word 82 shall be set to zero; release interrupt is not supported. Bit 8 of word 82 shall be set to zero; Service interrupt is not supported. Bit 9 of word 82 shall be set to zero; the Device Reset command is not supported. Bit 10 of word 82 shall be set to zero; the Host Protected Area feature set is not supported. Bit 11 of word 82 is obsolete. Bit 12 of word 82 shall be set to one; the CompactFlash™ Storage Card supports the Write Buffer command. Bit 13 of word 82 shall be set to one; the CompactFlash™ Storage Card supports the Read Buffer command. Bit 14 of word 82 shall be set to one; the CompactFlash™ Storage Card supports the NOP command.

Bit 15 of word 82 is obsolete. Bit 0 of word 83 shall be set to zero; the CompactFlash™ Storage Card does not support the Download Microcode command. Bit 1 of word 83 shall be set to zero; the CompactFlash™ Storage Card does not support the Read DMA Queued and Write DMA Queued commands. Bit 2 of word 83 shall be set to one; the CompactFlash™ Storage Card supports the CFA feature set. If bit 3 of word 83 is set to one, the CompactFlash™ Storage Card supports the Advanced Power Management feature set. Bit 4 of word 83 shall be set to zero; the CompactFlash™ Storage Card does not support the Removable Media Status feature set.

Words 85-87: Features/command sets enabled

Words 85, 86, and 87 shall indicate features/command sets enabled. The value 0000h or FFFFh was placed in each of these words by CompactFlash™ Storage Cards prior to ATA-4 and shall be interpreted by the host as meaning that features/command sets enabled are not indicated. Bits 1 through 15 of word 86 are reserved. Bits 0-13 of word 87 are reserved. Bit 14 of word 87 shall be set to one and bit 15 of word 87 shall be cleared to zero to provide indication that the features/command sets enabled words are valid. The values in these words should not be depended on by host implementers. Bit 0 of word 85 shall be set to zero; the SMART feature set is not enabled. If bit 1 of word 85 is set to one, the Security Mode feature set has been enabled via the Security Set Password command. Bit 2 of word 85 shall be set to zero; the Removable Media feature set is not supported. Bit 3 of word 85 shall be set to one; the Power Management feature set is supported. Bit 4 of word 85 shall be set to zero; the Packet Command feature set is not enabled. If bit 5 of word 85 is set to one, write cache is enabled. If bit 6 of word 85 is set to one, look-ahead is enabled. Bit 7 of word 85 shall be set to zero; release interrupt is not enabled. Bit 8 of word 85 shall be set to zero; Service interrupt is not enabled. Bit 9 of word 85 shall be set to zero; the Device Reset command is not supported. Bit 10 of word 85 shall be set to zero; the Host Protected Area feature set is not supported. Bit 11 of word 85 is obsolete. Bit 12 of word 85 shall be set to one; the CompactFlash™ Storage Card supports the Write Buffer command. Bit 13 of word 85 shall be set to one; the CompactFlash™ Storage Card supports the Read Buffer command. Bit 14 of word 85 shall be set to one; the

CompactFlash™ Storage Card supports the NOP command.

Bit 15 of word 85 is obsolete. Bit 0 of word 86 shall be set to zero; the CompactFlash™ Storage Card does not support the Download Microcode command. Bit 1 of word 86 shall be set to zero; the CompactFlash™ Storage Card does not support the Read DMA Queued and Write DMA Queued commands. If bit 2 of word 86 shall be set to one, the CompactFlash™ Storage Card supports the CFA feature set. If bit 3 of word 86 is set to one, the Advanced Power Management feature set has been enabled via the Set Features command. Bit 4 of word 86 shall be set to zero; the CompactFlash™ Storage Card does not support the Removable Media Status feature set.

Word 89: Time required for Security erase unit completion

Word 89 specifies the time required for the Security Erase Unit command to complete. This command shall be supported on CompactFlash™ Storage Cards that support security.

Value Time

0 Value not specified

1-254 (Value * 2) minute

255 >508 minutes

Word 90: Time required for Enhanced security erase unit completion

Word 90 specifies the time required for the Enhanced Security Erase Unit command to complete. This command shall be supported on CompactFlash™ Storage Cards that support security.

Value Time

0 Value not specified

1-254 (Value * 2) minutes

255 >508 minutes

Word 91: Advanced power management level value

Bits 7-0 of word 91 contain the current Advanced Power Management level setting.

Word 128: Security Status

Bit 8: Security Level

If set to 1, indicates that security mode is enabled and the security level is maximum.

If set to 0 and security mode is enabled, indicates that the security level is high.

Bit 5: Enhanced security erase unit feature supported

If set to 1, indicates that the Enhanced security erase unit feature set is supported.

Bit 4: Expire

If set to 1, indicates that the security count has expired and Security Unlock and Security Erase

Unit are command aborted until a power-on reset or hard reset.

Bit 3: Freeze

If set to 1, indicates that the security is Frozen.

Bit 2: Lock

If set to 1, indicates that the security is locked.

Bit 1: Enable/Disable

If set to 1, indicates that the security is enabled.

If set to 0, indicates that the security is disabled.

Bit 0: Capability If set to 1, indicates that CompactFlash™ Storage Card supports security mode feature set. If set to 0, indicates that CompactFlash™ Storage Card does not support security mode feature set.

Word 160: Power Requirement Description

This word is required for CompactFlash™ Storage Cards that support power mode 1.

Bit 15: VLD

If set to 1, indicates that this word contains a valid power requirement description.

If set to 0, indicates that this word does not contain a power requirement description.

Bit 14: RSV

This bit is reserved and must be 0.

Bit 13: -XP

If set to 1, indicates that the CompactFlash™ Storage Card does not have Power Level 1 commands.

If set to 0, indicates that the CompactFlash™ Storage Card has Power Level 1 commands

Bit 12: -XE

If set to 1, indicates that Power Level 1 commands are disabled.

If set to 0, indicates that Power Level 1 commands are enabled.

Bit 0-11: Maximum current

This field contains the CompactFlash™ Storage Card's maximum current in mA.

Word 162: Key Management Schemes Supported

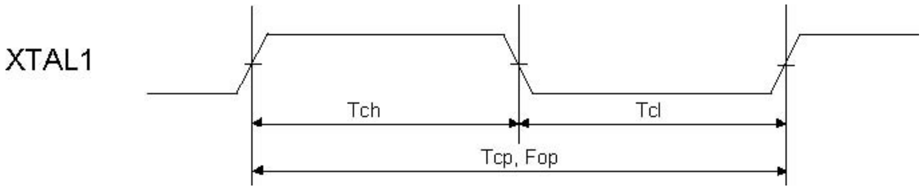
Bit 0: CPRM support

If set to 1, the device supports CPRM Scheme (Content Protection for Recordable Media)

If set to 0, the device does not support CPRM.

Bits 1-15 are reserved for future additional Key Management schemes.

Clock Input Timing



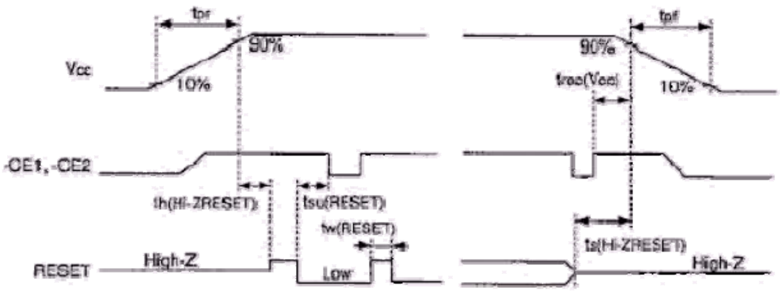
Parameter	Symbol	Min	Typ.	Max	Unit
Operating Speed	Fop	0	28.4	40	MHz
Clock Period	Tcp	25	35	-	ns
Clock High	Tch	12.5	17.5	-	ns
Clock Low	Tcl	12.5	17.5	-	ns

Notes:

1. The clock may be stopped indefinitely in either state.

2. The Tcp specification is used as a reference in other specifications.

Hard Reset Timing



Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Reset setup time	tsu(RESET)	100	—	—	ms	
-CE recover time	trec(VCC)	1	—	—	μs	
VCC rising up time	tpr	0.1	—	100	ms	
VCC falling down time	tpf	3	—	300	ms	
Reset pulse width	tw(RESET)	10	—	—	μs	
	th(HI-ZRESET)	1	—	—	ms	
	ts(HI-ZRESET)	0	—	—	ms	

Above technical information is based on industry standard data and tested to be reliable. However, makes no warranty, either expressed or implied, as to its accuracy and assumes no liability in connection with the use of this product. Reserves the right to make changes in specifications at any time without prior notice.

J. Product Model

J.1 Part number Decoder

Item	Controller	Capacity	Temperature range	Disk mode	Data Transfer mode
$X^1X^2X^3$	X^4X^5	$X^6X^7X^8X^9$	X^{10}	X^{11}	X^{12}
CFC	SU	016M: 16M Byte 032M: 32M Byte 064M: 64M Byte 128M: 128M Byte 256M: 256M Byte 512M: 512M Byte 001G: 1G Byte 002G: 2G Byte 004G: 4G Byte 008G: 8G Byte 016G: 16G Byte 032G: 32G Byte	C/I C: standard temp. I: wide temp.	F/R/A F: Fixed Disk Mode R: Removable Disk Mode A: Auto Detect Disk Mode	U/P U:UDMA 4 Mode P: PIO 4 Mode

J.2 Part number – Compactflash Card

Capacity	**Standard Temp.**	**Wide Temp.**
128MB	CFC-SU128MC$X^{11}X^{12}$	CFC-SU128MI$X^{11}X^{12}$
256MB	CFC-SU256MC$X^{11}X^{12}$	CFC-SU256MI$X^{11}X^{12}$
512MB	CFC-SU512MC$X^{11}X^{12}$	CFC-SU512MI$X^{11}X^{12}$
1GB	CFC-SU001GC$X^{11}X^{12}$	CFC-SU001GI$X^{11}X^{12}$
2GB	CFC-SU002GC$X^{11}X^{12}$	CFC-SU002GI$X^{11}X^{12}$
4GB	CFC-SU004GC$X^{11}X^{12}$	CFC-SU004GI$X^{11}X^{12}$
8GB	CFC-SU008GC$X^{11}X^{12}$	CFC-SU008GI$X^{11}X^{12}$
16GB	CFC-SU016GC$X^{11}X^{12}$	CFC-SU016GI$X^{11}X^{12}$
32GB	CFC-SU032GC$X^{11}X^{12}$	

Note:

X^{11}Disk mode

F: Fixed Disk Mode

R: Removable Disk Mode

A: Auto Detect Disk Mode

X^{12}Transfer mode

U:UDMA 4 Mode

P: PIO 4 Mode