Amtron Technology, Inc.

Industrial Grade 2.5” U.2 PCIe NVMe SSD

AC Series

Product Datasheet

V1.2

Table of Contents

1. INTRODUCTION

1.1. Description

Amtron industrial AC series U.2 PCIe SSD is designed with PCIe Gen3 x4 interface and is fully compliant with the standard 2.5-inch form factor and SFF-8639 connector. It can reach up to 3200 MB/s read and 1000 MB/s write high performance. These 2.5” U.2 PCIe SSD are offered in standard temperature grade (0°C to +70°C) and wide temperature grade (-40°C to +85°C). The memory capacities are available from 240GB to 7680GB (~8TB).

1.2. Product Features

- U.2 form factor
- PCI Express Base Version 3.1 and Compliant with NVMe 1.3
- PCIe Gen3 x 4 lane & backward compatible to PCIe Gen2 and Gen1
- RoHS compliant [Lead free]
- 3D Triple Level Cell (TLC) NAND Flash
- Capacity from 240GB up to 7680GB
- Hot-swapping
- High speed:
  - Read 3,200 MB/s max., Write 1,000 MB/s max.
- Endure severe thermal and dynamic environments
- Very low power consumption
- Power Loss Protection (optional feature)
- MTBF > 1,500,000 hours *****
- Support SMART and TRIM Command
- Controlled Bill of Materials (BOM)

***Note**: A lower MTBF is expected for higher capacity drives. To be conservative, the lowest MTBF is reported in this document

1.3. Product Overview

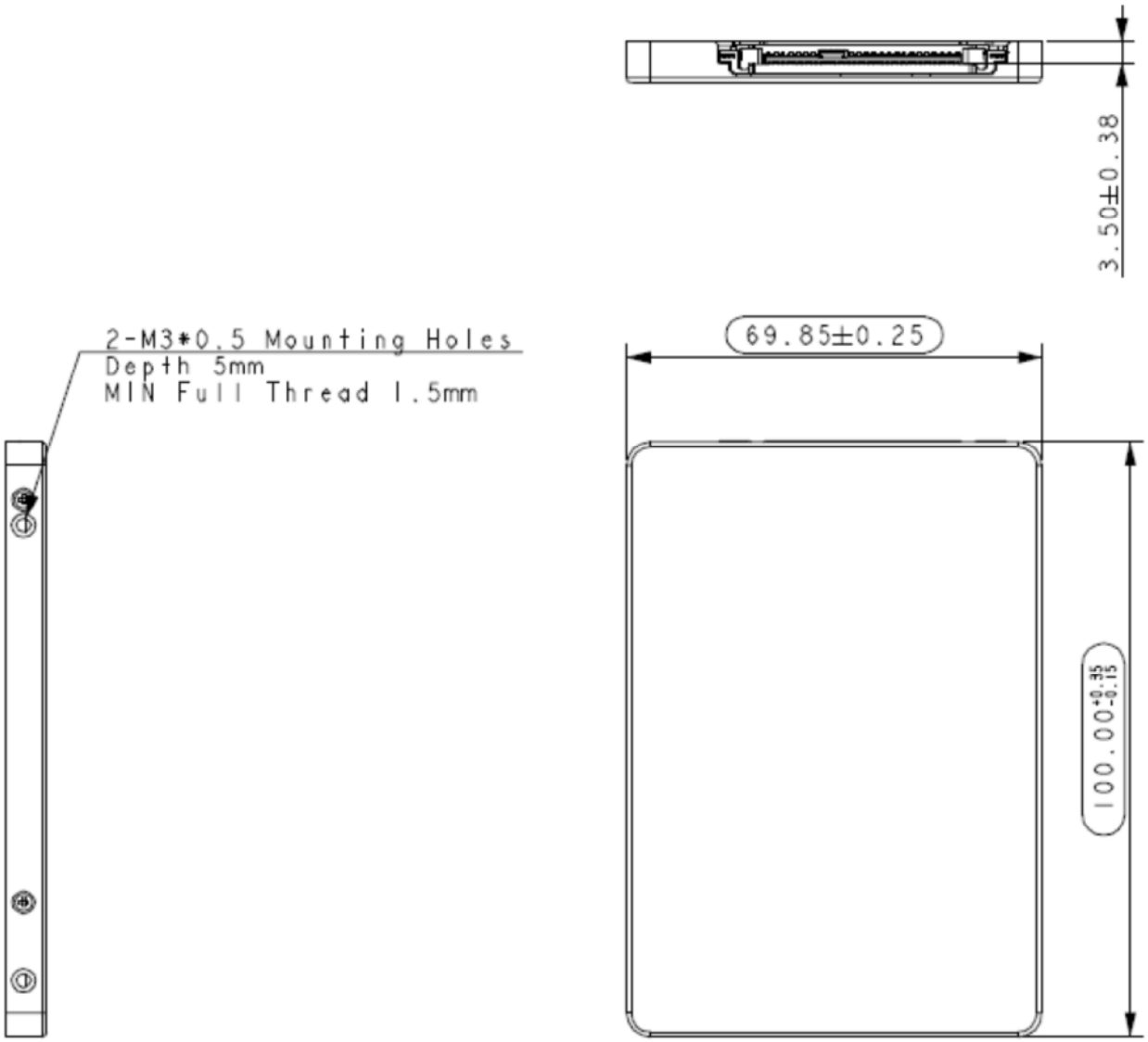
- **PCIe Interface**
  - NVMe PCIe Gen3 x4
- **Form Factor**
  - U.2
- **Compliance**
  - NVMe 1.3
  - PCI Express Base 3.1
- **Capacity**
  - 240GB up to 7.98TB
- **Flash Interface**
  - Flash Type: 3D TLC
  - Transfer rate up to 533 Mbps
  - Up to 16 pcs of BGA132/152 flash
- **Performance**
  - Read up to 3,200 MB/s
  - Write up to 1,000 MB/s
- **Reliability**
  - MTBF [1] > 1,500,000 hours
  - Uncorrectable Bit Error Rate(UBER) < 1 sector per 10^{16} bits read
- **Power Consumption** [2]
  - Active mode: < 9500mW
- **Advanced Flash Management**
  - Advanced Wear Leveling
  - Bad Block Management
  - TRIM
  - SMART
  - Over-Provision
- **Temperature Range**
  - Operation (standard): 0°C to 70°C
  - Operation (wide): -40°C to 85°C
  - Storage: -40°C to 85°C
- **Features Support List**
  - End to end data path protection
  - Thermal throttling
  - SmartECC™
  - SmartRefresh™
  - Drive log
  - Support of AES/TCG OPAL[3] (Optional)
- **Compliant**
  - RoHS
- **Hardware Support**
  - Power Loss Protection (Optional)

Note:

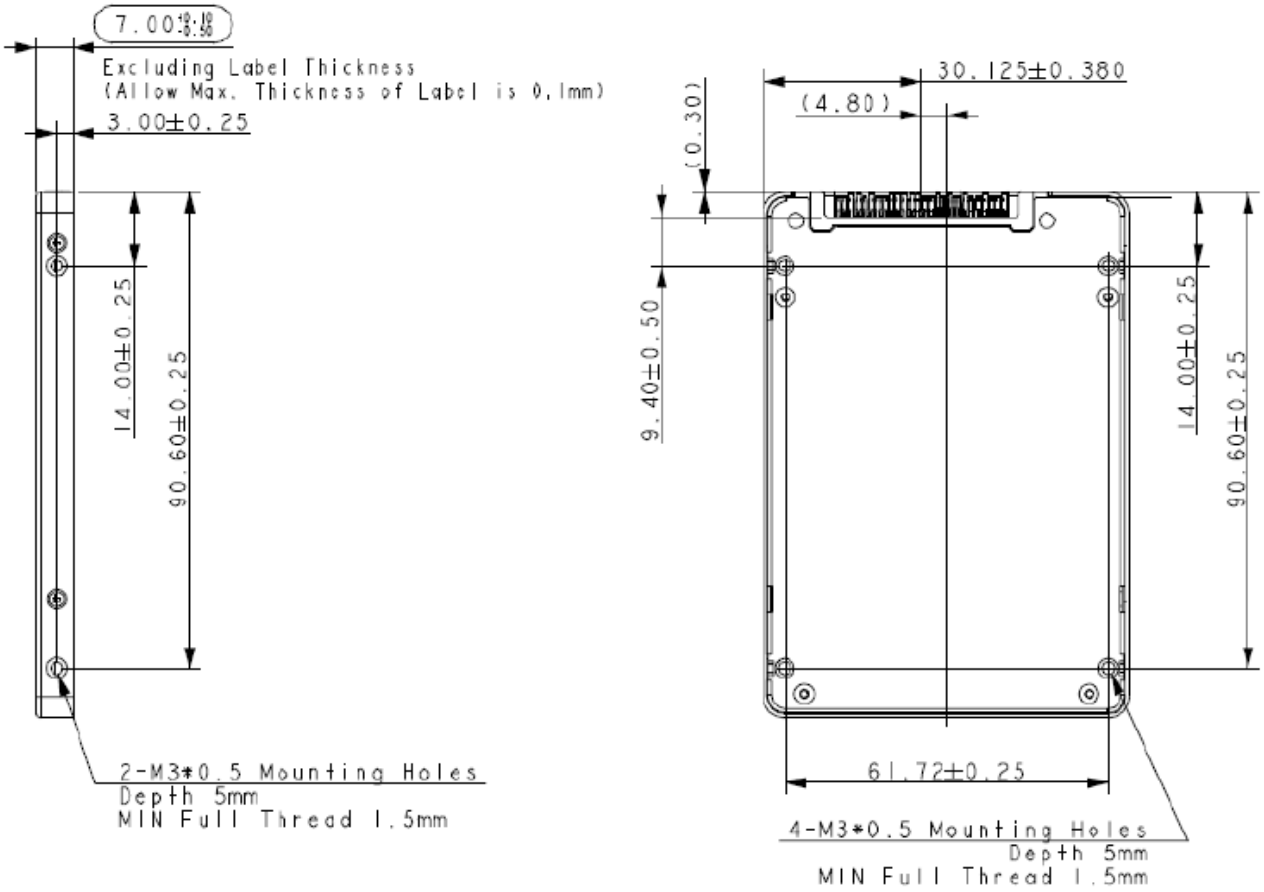
1. **MTBF** (mean time between failures) is a measure of how reliable a hardware product is. Its value represents the average time between a failure repair and the next failure. The unit of MTBF is typically in hours. The higher the MTBF value, the higher the reliability of the product. Please note that a lower MTBF is expected for higher capacity drives. To be conservative, the lowest MTBF is reported in this document.
2. See Section 4.2 "Power Consumption" for details.
3. Optional features support by a separate firmware version. See Section 8 "Part Number Decoder".

1.4. Product Dimension

100.00mm (L) x 69.85mm (W) x 7.00mm (H)



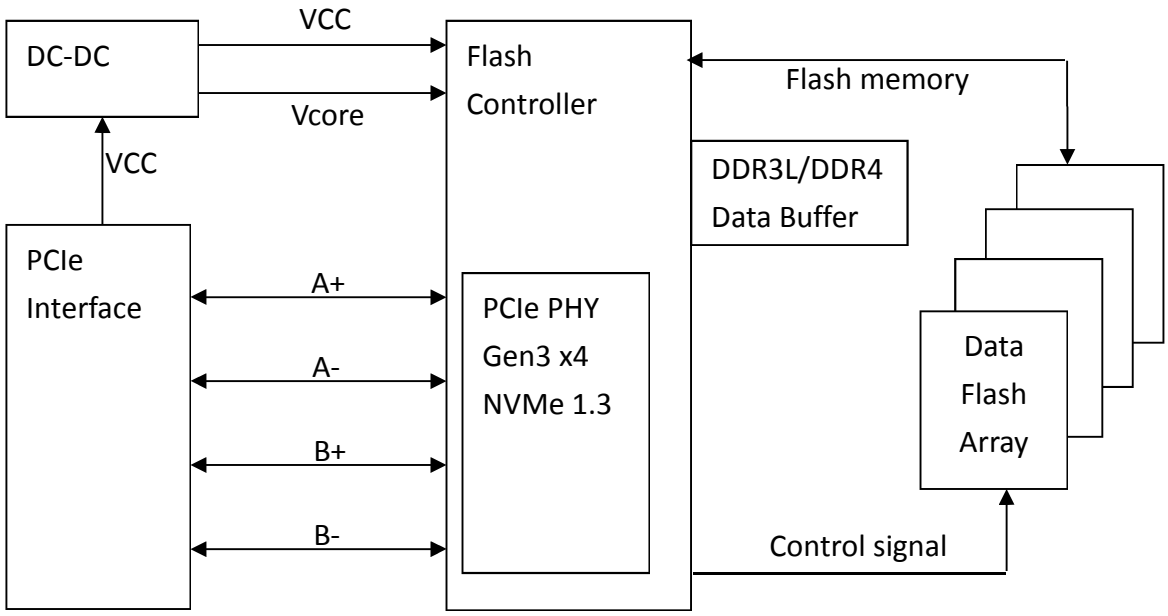
Top View



Bottom View

Notes:
1.Common tolerance refers to class (B).
2. ( ) are critical dimensions.
3.All of dimension except critical dimension, please perform real assembly.
4.( ) is reference dimension.

1.5. Block Diagram



U.2 PCIe SSD Block Diagram

2. PRODUCT SPECIFICATIONS

2.1. Specifications

- **Capacity**
  - 240GB up to 7680GB
- **Electrical/Physical Interface**
  - PCI Express Base Ver 3.1
  - Compliant with NVMe 1.3
  - PCIe Gen3 x 4 lane & backward compatible to PCIe Gen2 and Gen1
- **Supported NAND Flash**
  - Support Toshiba BiCS3 TLC
  - Support up to 16pcs of BGA132/152 flash
- **ECC Scheme**
  - Applies LDPC of ECC algorithm
- **Sector Size Support**
  - 512Bytes
  - 4KB
- **UART / GPIO**
- **Support SMART and TRIM commands**
- **Support Hardware Power Loss Protection (Optional)**
  - Protect data loss, even the last data, during write process when power sudden off.
  - Add-on Polymer Tantalum Capacitors hold-up several milliseconds to keep DRAM data write to NAND Flash.

- **LBA Range**
  - IDEMA standard

Capacity	Total Sectors (LBA)	User Data Size
240GB	468,862,128	Depended on file management
480GB	937,703,088	
960GB	1,875,385,008	
1920GB	3,750,748,848	
3840GB	7,501,476,528	
7680GB	15,002,931,888	

- **Performance**
  - **BiCS3 TLC**

Capacity	Flash Structure	Flash Type	Sequential		Random	
			Read (MB/s)	Write (MB/s)	Read (IOPS)	Write (IOPS)
240GB	64GB x 4	BiCS3, BGA	3,000	340	100K	13K
480GB	64GB x 8	BiCS3, BGA	3,000	520	200K	20K
960GB	128GB x 8	BiCS3, BGA	3,200	1,000	360K	25K
1920GB	128GB x 16	BiCS3, BGA	3,200	1,000	360K	28K
3840GB	256GB x 16	BiCS3, BGA	2,900	970	400K	30K
7680GB	512GB x 16	BiCS3, BGA	2,900	970	400K	30K

Notes:

1. The performance was estimated based on Toshiba BiCS3 TLC NAND flash.
2. Performance may differ according to flash configuration and platform.
3. The table above is for reference only. Any criteria for accepting goods shall be discussed based on different flash configurations.
4. Performance is measured with the follow conditions

(a) CrystalDiskMark 6.0, 1GB range, QD=32, Thread=1

(b) IOMeter, 4K data size, QD=256

- **TBW (Terabytes Written)**
  - **BiCS3 TLC**

Capacity	Flash Type	TBW
240GB	BiCS3 TLC	394
480GB	BiCS3 TLC	806
960GB	BiCS3 TLC	1,586
1920GB	BiCS3 TLC	3,031
3840GB	BiCS3 TLC	6,286
7680GB	BiCS3 TLC	12,044

Notes:

1. Samples were built using Toshiba BiCS3 TLC NAND flash.
2. The test followed JEDEC218/219A client endurance workload.
3. TBW may differ according to flash configuration and platform.

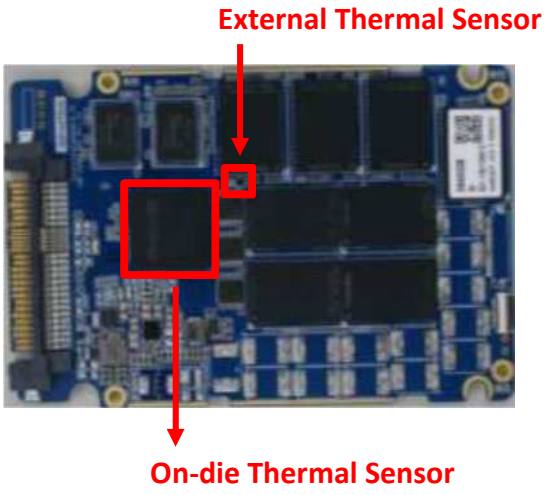
2.2. Thermal Throttling

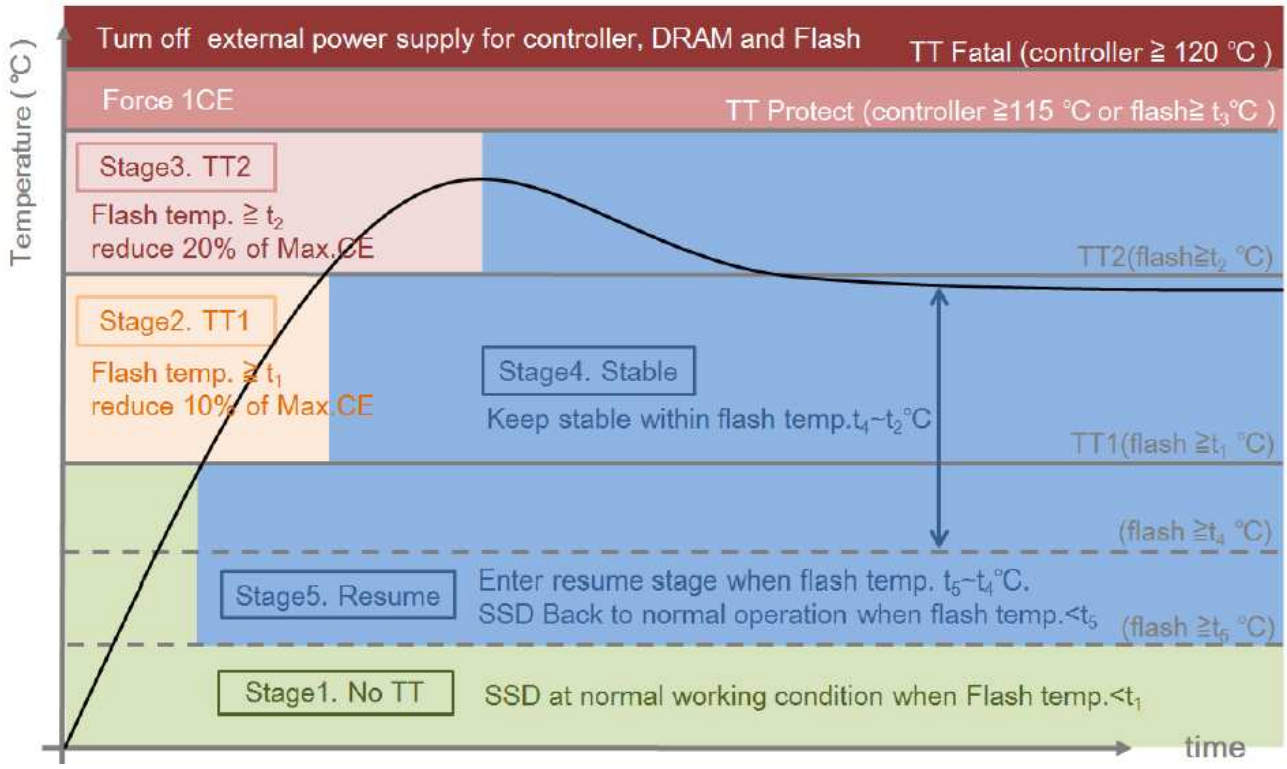
The purpose of thermal throttling is to prevent any components in a SSD from over-heating during read and write operations. The controller is designed with an on-die thermal sensor and with its accuracy, firmware can apply different levels of throttling to achieve the purpose of protection efficiently and proactively via S.M.A.R.T. reading.

- **SSD Configuration:**
  - Example 480GB SSD: (BiCS3 256Gb x 2CE) x 8pcs BGA132/152, total 16CE
  - CE = Chip Enable pins, max CE = All 16CE enabled. Total CE numbers depends on SSD configuration

- **Purpose of Thermal Throttling:**
  - In order to keep the optimal performance in the safe range of the temperature.

- **Thermal sensors:**
  - We have external thermal sensor & on-die thermal sensor (internal controller) to detect temperature. There is 1pcs external thermal sensor on PCB, the position depends on different form factor (The thermal sensor is shown below. The picture is for reference only).
  - External thermal sensor would detect flash temperature; On-die thermal sensor detect controller temperature.





	Operation temp. of Normal-temp. grade: 0-70°C	Operation temp. of Wide-temp. grade: -40-85°C
t_1	68°C	82°C
t_2	70°C	85°C
t_3	80°C	95°C
t_4	64°C	78°C
t_5	60°C	74°C

Notes:

1. TT shown on Figure 2-1 means "Thermal Throttling".
2. CE = Chip Enable.
3. temp. = temperature

2.3. MTBF

MTBF (mean time between failures) is a measure of how reliable a hardware product is. Its value represents the average time between a failure repair and the next failure. The unit of MTBF is typically in hours. The

higher the MTBF value, the higher the reliability of the product. The MTBF calculated in this document is based on a software tool, Relex 7.3 . Please note that a lower MTBF is expected for higher capacity drives. To be conservative, the lowest MTBF is reported in this document.

3. ENVIRONMENTAL SPECIFICATIONS

3.1. Environmental Conditions

3.1.1. Temperature and Humidity

- Operational (Standard grade): 0°C to 70°C
- Operational (Wide grade): -40°C to 85°C
- Storage: -40°C to 85°C

■ **High Temperature Test Condition**

	Temperature	Humidity
Operation	70°C/85°C	0% RH
Storage	85°C	0% RH

■ **Low Temperature Test Condition**

	Temperature	Humidity
Operation	0°C/-40°C	0% RH
Storage	-40°C	0% RH

■ **High Humidity Test Condition**

	Temperature	Humidity
Operation	40°C	90% RH
Storage	40°C	93% RH

■ **Temperature Cycle Test**

	Temperature
Operation	0°C/-40°C
	70°C/85°C
Storage	-40°C
	85°C

Notes:

1. Operation temperature is measured by device temperature sensor. Airflow is suggested and it will allow device to be operated at appropriate temperature for each component during heavy workloads environment.
2. Operation temperature shows in case temperature not ambient temperature.

3.1.2. Shock

■ **Shock Specification**

	Acceleration Force
Non-Operational	1500G
Operational	1500G

3.1.3. Vibration

■ **Vibration Specification**

	Condition	
	Frequency/Displacement	**Frequency/Acceleration**
Non-Operational	20Hz~80Hz/1.52mm	80Hz~2000Hz/20G

3.1.4. Drop

■ **Drop Specification**

	Height of Drop	Number of Drop
Non-operational	80cm free fall	6 face of each unit

3.1.5. Bending

■ **Bending Specification**

	Force	Action
Non-operational	≥ 20N	Hold 1min/5times

3.1.6. Electrostatic Discharge (ESD)

Specification	+/- 4KV
EN 55024, CISPR 24 EN 61000-4-2 and IEC 61000-4-2	Device functions are affected, but EUT will be back to its normal or operational state automatically.

3.1.7. EMI Compliance

Specification
EN 55032, CISPR 32 (CE)
AS/NZS CISPR 32 (CE)
ANSI C63.4 (FCC)
VCCI-CISPR 32 (VCCI)
CNS 13438 (BSMI)

3.2. Certification & Compliance

- RoHS

4. ELECTRICAL SPECIFICATIONS

4.1. Supply Voltage

Parameter	Rating
Operating Voltage	12V

4.2. Power Consumption

- Power consumption of U.2 PCIe SSD

Capacity	Flash Type	CE#	Read (mW)	Write (mW)
240GB	64GB x4, Bics3 TLC, BGA	8	5,600	3,200
480GB	64GB x8, Bics3 TLC, BGA	16	6,100	3,400
960GB	128B x8, Bics3 TLC, BGA	32	6,300	4,600
1920GB	128GB x16, Bics3 TLC, BGA	32	8,000	5,500
3840GB	256GB x16, Bics3 TLC, BGA	64	8,500	6,000
7680GB	512GB x16, Bics3 TLC, BGA	64	9,500	6,600

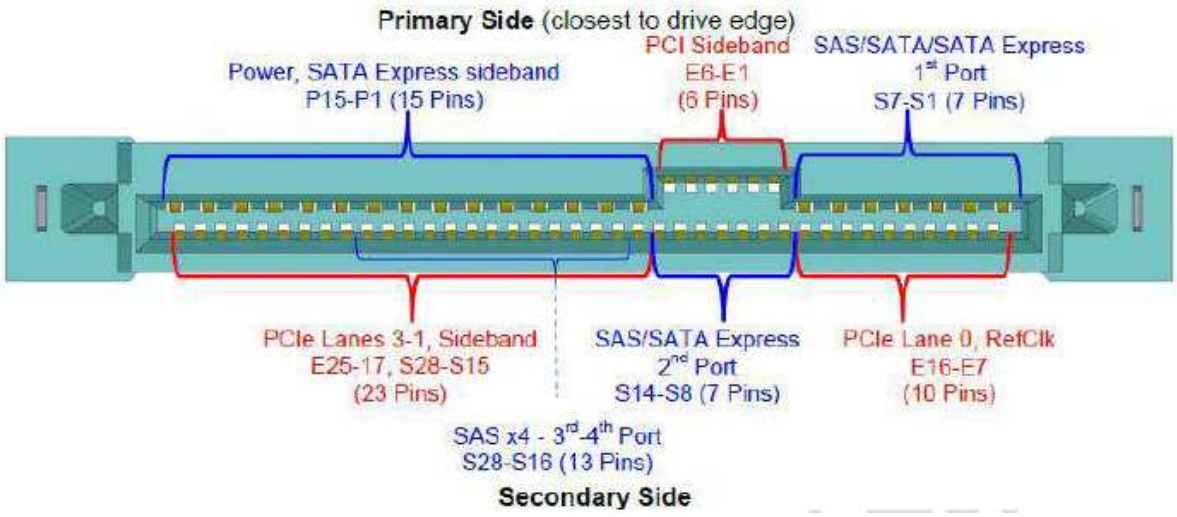
Unit: mW

Notes

1. Based on ambient temperature.
2. The average value of power consumption is achieved based on 100% conversion efficiency.
3. Sequential R/W is measured while testing 1GB sequential R/W 5 times by CyrstalDiskMark.
4. Power Consumption may differ according to flash configuration and platform.
5. The measured power voltage is 12V.

5. INTERFACE

5.1. Pin Assignment and Descriptions



The follow table defines the signal assignment of the 2.5” U.2 PCIe SSD SFF-8639 Connector Pin Assignment and Descriptions.

Pin #	Name	Type	Description
P1	WAKE#	Input	Signal for Link reactivation
P2	-	-	Outside scope of this specification
P3	CLKREQ#	Bi-Dir	Clock request
P4	IfDet#	Input	Interface Type Detect
P5	Ground	Ground	Ground
P6	Ground	Ground	Ground
P7	-	-	Outside scope of this specification
P8	-	-	Outside scope of this specification
P9	-	-	Outside scope of this specification
P10	PRSNT#	Input	Presence detect
P11	Activity	Input	
P12	Ground	Ground	Ground
P13	+12V Precharge	Power	+12V Precharge power for SFF-8639 module
P14	+12V	Power	+12V power for SFF-8639 module
P15	+12V	Power	+12V power for SFF-8639 module
S1	Ground	Ground	Ground
S2	-	-	Outside scope of this specification
S3	-	-	Outside scope of this specification

Pin #	Name	Type	Description
S4	Ground	Ground	Ground
S5	-	-	Outside scope of this specification
S6	-	-	Outside scope of this specification
S7	Ground	Ground	Ground
S8	Ground	Ground	Ground
S9	-	-	Outside scope of this specification
S10	-	-	Outside scope of this specification
S11	Ground	Ground	Ground
S12	-	-	Outside scope of this specification
S13	-	-	Outside scope of this specification
S14	Ground	Ground	Ground
S15	Reserved	-	Reserved
S16	Ground	Ground	Ground
S17	PETp1	Diff-Pair	Transmitter differential pair, Lane 1
S18	PETn1	Diff-Pair	Transmitter differential pair, Lane 1
S19	Ground	Ground	Ground
S20	PERn1	Diff-Pair	Receiver differential pair, Lane 1
S21	PERp1	Diff-Pair	Receiver differential pair, Lane 1
S22	Ground	Ground	Ground
S23	PETp2	Diff-Pair	Transmitter differential pair, Lane 2
S24	PETn2	Diff-Pair	Transmitter differential pair, Lane 2
S25	Ground	Ground	Ground
S26	PERn2	Diff-Pair	Receiver differential pair, Lane 2
S27	PERp2	Diff-Pair	Receiver differential pair, Lane 2
S28	Ground	Ground	Ground
E1	REFCLKB+	Diff-Pair	Reference clock (differential pair) for second X2 port
E2	REFCLKB-	Diff-Pair	Reference clock (differential pair) for second X2 port
E3	+3.3 Vaux	Power	3.3 V auxiliary power
E4	PERSTB#	Output	Fundamental reset for second X2 port
E5	PERST#	Output	Fundamental reset (if dual-port enabled, first X2 port)
E6	Reserved	-	Reserved
E7	REFCLK+	Diff-Pair	Reference clock (if dual-port enabled, first X2 port)
E8	REFCLK-	Diff-Pair	Reference clock (if dual-port enabled, first X2 port)
E9	Ground	Ground	Ground
E10	PETp0	Diff-Pair	Transmitter differential pair, Lane 0

Pin #	Name	Type	Description
E11	PETn0	Diff-Pair	Transmitter differential pair, Lane 0
E12	Ground	Ground	Ground
E13	PERn0	Diff-Pair	Receiver differential pair, Lane 0
E14	PERp0	Diff-Pair	Receiver differential pair, Lane 0
E15	Ground	Ground	Ground
E16	Reserved	-	Reserved
E17	PETp3	Diff-Pair	Transmitter differential pair, Lane 3
E18	PETn3	Diff-Pair	Transmitter differential pair, Lane 3
E19	Ground	Ground	Ground
E20	PERn3	Diff-Pair	Receiver differential pair, Lane 3
E21	PERp3	Diff-Pair	Receiver differential pair, Lane 3
E22	Ground	Ground	Ground
E23	SMCLK	Bi-Dir	SMBus (System Management Bus) clock
E24	SMDAT	Bi-Dir	SMBus (System Management Bus) data
E25	DualPortEn#	Output	Dual-port Enable

6. SUPPORTED COMMANDS

6.1. NVMe Command List

Table 6-1 Admin Commands

Op-Code	O/M	Command Description
00h	M	Delete I/O Submission Queue
01h	M	Create I/O Submission Queue
02h	M	Get Log Page
04h	M	Delete I/O Completion Queue
05h	M	Create I/O Completion Queue
06h	M	Identify
08h	M	Abort
09h	M	Set Features
0Ah	M	Get Features
0Ch	M	Asynchronous Event Request
10h	O	Firmware Activate
11h	O	Firmware Image Download
14h	O	Device Self-test
80h	O	Format NVM
81h	O	Security Send
82h	O	Security Receive
84h	O	Sanitize

Table 6-2 I/O Commands

Op-Code	O/M	Command Description
00h	O	Flush
01h	O	Write
02h	O	Read
04h	O	Write Uncorrectable
05h	O	Compare
08h	O	Write Zeroes
09h	O	Dataset Management

Table 6-3 Set Feature Commands

Op-Code	O/M	Command Description
00h		Reserved
01h	M	Arbitration
02h	M	Power Management
03h	O	LBA Range Type
04h	M	Temperature Threshold
05h	M	Error Recovery
06h	O	Volatile Write Cache
07h	M	Number of Queues
08h	M	Interrupt Coalescing
09h	M	Interrupt Vector Configuration
0Ah	M	Write Atomicity Normal
0Bh	M	Asynchronous Event Configuration
0Ch	O	Autonomous Power State Transition
0Dh	O	Host Memory Buffer
0Eh	O	Timestamp
10h	O	Host Controlled Thermal Management
11h	O	Non-Operational Power State Config
0Eh – 7Dh		Reserved
80h	O	Software Progress Marker

Table 6-4 Get Log Page Commands

Op-Code	O/M	Command Description
00h		Reserved
01h	M	Error Information
02h	M	SMART / Health Information
03h	M	Firmware Slot Information
04h	O	Changed Namespace List
06h	O	Device Self-test
09h – 7Fh		Reserved
81h	O	Sanitize Status
82h - FFh		Reserved

6.2. Identify Device Data

The following table details the sector data returned by the IDENTIFY DEVICE command.

■ Identify Controller Data Structure

Bytes	O/M	Default Value	Description
01:00	M	0x1987	PCI Vendor ID (VID)
03:02	M	0x1987	PCI Subsystem Vendor ID (SSVID)
23:04	M	TBD	Serial Number (SN)
63:24	M	TBD	Model Number (MN)
71:64	M	TBD	Firmware Revision (FR)
72	M	0x01	Recommended Arbitration Burst (RAB)
75:73	M	TBD *	IEEE OUI Identifier (IEEE)
76	O	0x00	Controller Multi-Path I/O and Namespace Sharing Capabilities (CMIC)
77	M	0x09	Maximum Data Transfer Size (MDTS)
79:78	M	0x0001	Controller ID (CNTLID)
83:80	M	0x00010300	Version (VER)
87:84	M	0x001E8480(2sec)	RTD3 Resume Latency (RTD3R)
91:88	M	0x00989680(10sec)	RTD3 Entry Latency (RTD3E)
95:92	M	0x00000300	Optional Asynchronous Events Supported (OAES)
99:96	M	0x0002	Controller Attributes (CTRATT)
239:100	-	0x00	Reserved
255:240	-	0x00	Refer to the NVMe Management Interface Specification for definition
257:256	M	0x0017	Optional Admin Command Support (OACS)
258	M	0x03	Abort Command Limit (ACL)
259	M	0x03	Asynchronous Event Request Limit (AERL)
260	M	0x1F	Firmware Updates (FRMW)
261	M	0x0C	Log Page Attributes (LPA)
262	M	0x3E	Error Log Page Entries (ELPE)
263	M	4	Number of Power States Support (NPSS)
264	M	0x01	Admin Vendor Specific Command Configuration (AVSCC)
265	O	0x01	Autonomous Power State Transition Attributes (APSTA)
267:266	M	0x0157 (70C)	Warning Composite Temperature Threshold (WCTEMP)
269:268	M	0x0161 (80C)	Critical Composite Temperature Threshold (CCTEMP)
271:270	O	0x0000 (No report)	Maximum Time for Firmware Activation (MTFA)
275:272	O	0x00000000	Host Memory Buffer Preferred Size (HMPRE)
279:276	O	0x00000000	Host Memory Buffer Minimum Size (HMMIN)

Bytes	O/M	Default Value	Description
295:280	O	**	Total NVM Capacity (TNVMCAP)
311:296	O	**	Unallocated NVM Capacity (UNVMCAP)
315:312	O	0x00000000	Replay Protected Memory Block Support (RPMBS)
511:316	-	Non-zero	Reserved
NVM Command Set Attributes			
512	M	0x66	Submission Queue Entry Size (SQES)
513	M	0x44	Completion Queue Entry Size (CQES)
515:514	-	0x0000	Reserved
519:516	M	0x00000001	Number of Namespaces (NN)
521:520	M	0x001F	Optional NVM Command Support (ONCS)
523:522	M	0x0000	Fused Operation Support (FUSES)
524	M	0x00	Format NVM Attributes (FNA)
525	M	0x01	Volatile Write Cache (VWC)
527:526	M	TBD	Atomic Write Unit Normal (AWUN)
529:528	M	TBD	Atomic Write Unit Power Fail (AWUPF)
530	M	0x01	NVM Vendor Specific Command Configuration (NVSCC)
531	-	0x00	Reserved
533:532	O	0x0000	Atomic Compare & Write Unit (ACWU)
535:534	-	0x0000	Reserved
539:536	O	0x00000000	SGL Support (SGLS)
703:540	-	0x00	Reserved
IO Command Set Attributes			
2047:704	-	0x00	Reserved
2079:2048	M	TBD	Power State 0 Descriptor (PSD0)
2111:2080	O	0x00	Power State 1 Descriptor (PSD1)
2143:2112	O	0x00	Power State 2 Descriptor (PSD2)
2175:2144	O	0x00	Power State 3 Descriptor (PSD3)
2207:2176	O	0x00	Power State 4 Descriptor (PSD4)
2239:2208	O	0x00	Power State 5 Descriptor (PSD5)
2271:2240	O	0x00	Power State 6 Descriptor (PSD6)
2303:2272	O	0x00	Power State 7 Descriptor (PSD7)
2335:2304	O	0x00	Power State 8 Descriptor (PSD8)
2367:2336	O	0x00	Power State 9 Descriptor (PSD9)
2399:2368	O	0x00	Power State 10 Descriptor (PSD10)
2431:2400	O	0x00	Power State 11 Descriptor (PSD11)

Bytes	O/M	Default Value	Description
2463:2432	O	0x00	Power State 12 Descriptor (PSD12)
2495:2464	O	0x00	Power State 13 Descriptor (PSD13)
2527:2496	O	0x00	Power State 14 Descriptor (PSD14)
2559:2528	O	0x00	Power State 15 Descriptor (PSD15)
2591:2560	O	0x00	Power State 16 Descriptor (PSD16)
2623:2592	O	0x00	Power State 17 Descriptor (PSD17)
2655:2624	O	0x00	Power State 18 Descriptor (PSD18)
2687:2656	O	0x00	Power State 19 Descriptor (PSD19)
2719:2688	O	0x00	Power State 20 Descriptor (PSD20)
2751:2720	O	0x00	Power State 21 Descriptor (PSD21)
2783:2752	O	0x00	Power State 22 Descriptor (PSD22)
2815:2784	O	0x00	Power State 23 Descriptor (PSD23)
2847:2816	O	0x00	Power State 24 Descriptor (PSD24)
2879:2848	O	0x00	Power State 25 Descriptor (PSD25)
2911:2880	O	0x00	Power State26 Descriptor (PSD26)
2943:2912	O	0x00	Power State 27 Descriptor (PSD27)
2975:2944	O	0x00	Power State 28 Descriptor (PSD28)
3007:2976	O	0x00	Power State 29 Descriptor (PSD29)
3039:3008	O	0x00	Power State 30 Descriptor (PSD30)
3071:3040	O	0x00	Power State 31 Descriptor (PSD31)
Vendor Specific			
4095:3072	O	Vendor Reserved	Vendor Specific (VS)

***** The OUI shall be a valid IEEE/RAC assigned identifier that may be registered at http://standards.ieee.org/develop/regauth/oui/public.html.

****** Depends on the using of capacity

■ Identify Namespace Data Structure & NVM Command Set Specific

Bytes	O/M	Default Value	Description
7:0	M	TBD*	Namespace Size (NSZE)
15:8	M	TBD*	Namespace Capacity (NCAP)
23:16	M	TBD*	Namespace Utilization (NUSE)
24	M	0x00	Namespace Features (NSFEAT)
25	M	0x01	Number of LBA Formats (NLBAF)
26	M	0x00	Formatted LBA Size (FLBAS)
27	M	0x00	Metadata Capabilities (MC)
28	M	0x00	End-to-end Data Protection Capabilities (DPC)
29	M	0x00	End-to-end Data Protection Type Settings (DPS)
30	O	0x00	Namespace Multi-path I/O and Namespace Sharing Capabilities (NMIC)
31	O	0x00	Reservation Capabilities (RESCAP)
32	O	0x00	Format Progress Indicator (FPI)
33	-	0x00	Reserved
35:34	O	0x0000	Namespace Atomic Write Unit Normal (NAWUN)
37:36	O	0x0000	Namespace Atomic Write Unit Power Fail (NAWUPF)
39:38	O	0x0000	Namespace Atomic Compare & Write Unit (NACWU)
41:40	O	0x0000	Namespace Atomic Boundary Size Normal (NABSN)
43:42	O	0x0000	Namespace Atomic Boundary Offset (NABO)
45:44	O	0x0000	Namespace Atomic Boundary Size Power Fail (NABSPF)
47:46	-	0x0000	Reserved
63:48	O	0x00	NVM Capacity (NVMCAP)
103:64	-	0x00	Reserved
119:104	O	TBD **	Namespace Globally Unique Identifier (NGUID)
127:120	O	TBD **	IEEE Extended Unique Identifier (EUI64)
131:128	M	0x02090000	LBA Format 0 Support (LBAF0)
135:132	O	0x00000000	LBA Format 1 Support (LBAF1)
139:136	O	0x00000000	LBA Format 2 Support (LBAF2)
143:140	O	0x00000000	LBA Format 3 Support (LBAF3)
147:144	O	0x00000000	LBA Format 4 Support (LBAF4)
151:148	O	0x00000000	LBA Format 5 Support (LBAF5)
155:152	O	0x00000000	LBA Format 6 Support (LBAF6)
159:156	O	0x00000000	LBA Format 7 Support (LBAF7)
163:160	O	0x00000000	LBA Format 8 Support (LBAF8)
167:164	O	0x00000000	LBA Format 9 Support (LBAF9)

Bytes	O/M	Default Value	Description
171:168	O	0x00000000	LBA Format 10 Support (LBAF10)
175:172	O	0x00000000	LBA Format 11 Support (LBAF11)
179:176	O	0x00000000	LBA Format 12 Support (LBAF12)
183:180	O	0x00000000	LBA Format 13 Support (LBAF13)
187:184	O	0x00000000	LBA Format 14 Support (LBAF14)
191:188	O	0x00000000	LBA Format 15 Support (LBAF15)
383:192	-	0x00	Reserved
4095:384	O	0x00	Vendor Specific (VS)

***** See IDEMA SPEC

****** See IEEE EUI-64 SPEC

■ **List of Identify Namespace Data Structure for Each Capacity**

Capacity (GB)	Byte[7:0]: Namespace Size (NSZE)
240	1BF244B0h
480	37E436B0h
960	6FC81AB0h
1920	DF8FE2B0h
3840	1BF1F72B0h
7680	37E3E92B0h

6.3. SMART Attributes

■ **SMART Attributes (Log Identifier 02h)**

Bytes Index	Bytes	Description
[0]	1	Critical Warning
[2:1]	2	Composite Temperature
[3]	1	Available Spare
[4]	1	Available Spare Threshold
[5]	1	Percentage Used
[31:6]	26	Reserved
[47:32]	16	Data Units Read
[63:48]	16	Data Units Written
[79:64]	16	Host Read Commands
[95:80]	16	Host Write Commands
[111:96]	16	Controller Busy Time
[127:112]	16	Power Cycles
[143:128]	16	Power On Hours
[159:144]	16	Unsafe Shutdowns
[175:160]	16	Media and Data Integrity Errors
[191:176]	16	Number of Error Information Log Entries
[195:192]	4	Warning Composite Temperature Time
[199:196]	4	Critical Composite Temperature Time
[201:200]	2	Temperature Sensor 1 (Current Temperature)
[203:202]	2	Temperature Sensor 2 (N/A)
[205:204]	2	Temperature Sensor 3 (N/A)
[207:206]	2	Temperature Sensor 4 (N/A)
[209:208]	2	Temperature Sensor 5 (N/A)
[211:210]	2	Temperature Sensor 6 (N/A)
[213:212]	2	Temperature Sensor 7 (N/A)
[215:214]	2	Temperature Sensor 8 (N/A)
[511:216]	296	Reserved

7. ACRONYMS

Acronym	Definition
AES	Advanced Encryption Standard
APST	Autonomous Power State Transition
ASPM	Active States Power Management
ECC	Error Correcting Code
DDR	Double Data Rate (SDRAM)
LBA	Logical Block Addressing
LDPC	Low-Density Parity Check
MTBF	Mean Time Between Failures
NVMe	Non-Volatile Memory Express
OPAL	Open Physics Abstraction Layer
PCIe	PCI Express / Peripheral Component Interconnect Express
PLP	Power Loss Protection
SMART	Self-Monitoring, Analysis and Reporting Technology
TCG	Trusted Computing Group
TLC	Tipple Level Cell
UBER	Uncorrectable Bit Error Rate

8. PART NUMBER DECODER

U2P-ACX^{1}X^{2}X^{3}X^{4}X^{5}X^{6}X^{7}X^{8}X^{9}

Item	Series	Capacity	NAND Flash & Temperature Grade	Option
		X^{1} X^{2} X^{3} X^{4} X^{5} X^{6}	**X^{7}**	**X^{8} X^{9}**
U2P	**AC**	**0240GB** (240GB) **0480GB** (480GB) **0960GB** (960GB) **1920GB** (1.92TB) **3840GB** (3.84TB) **7680GB** (7.68TB)	**A** : 3D TLC , Standard (0˚C to +70˚C) **B** : 3D TLC , Wide (-40˚C to +85˚C)	See below

X^{8} X^{9} (Reserved for specific requirement)

Blank: Standard
06: Conformal Coating (CC)
31: AES+OPAL (PSID code)
32: PLP+AES+OPAL (PSID code)