Revision History

Rev	Date	Details
A	February 29, 2008	Release of SMART PC data sheet w/SM223 controller

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64MB – 32GB Industrial Grade XceedAT Card

1 General Description

1.1 Overview

SMART is a leading independent manufacturer of memory and embedded modular sub-systems inclusive of board-level through systems level design, manufacturing, test and fulfillment services. SMART offers more than 500 standard and custom products to leading OEMs in the computer, industrial, networking and telecommunications industries worldwide.

SMART's Industrial Grade XceedAT product offering is specifically targeted at the needs of OEM markets such as networking, telecommunications and data communications applications. SMART's XceedAT products are also a natural fit for mobile and embedded computing, medical, automotive and industrial applications.

SMART's Industrial Grade XceedAT products offer reliable high performance operation in an industry standard Type 1 ultrasonic welded PC housing. They are available in capacities from 64MB to 32GB and can operate in either 3.3V or 5V hosts.
SMART Industrial Grade XceedAT products offer an advanced static wear-leveling algorithm for extending the lifespan of the products for demanding applications. SMART Industrial Grade Flash products ensure repeatable, reliable operation in Industrial OEM applications.
SMART further increases the reliability of its Industrial Grade XceedAT product offering - yielding greater than 2 Million Program/Erase cycles for most applications - by using Single Level Cell NAND Flash technology which betters comparable Multi Level Cell technology by a factor of 10X in reliability and 2X in speed.
SMART has built its foundation by providing proven technology and quality products to the most demanding Fortune 100 OEMs. SMART engineers its products to perform at the highest degree of reliability & compatibility while backing these products with outstanding services and technology expertise.

1.2 Features

- PC Card Standard Release 8 Compliant
- Capacity Range 64MB to 32GB
- CIS (Card Information Structure) programmed into 256 Bytes of Attribute Memory
- Low Power Dissipation
  - High Performance Read Current: 60 mA
  - High Performance Write Current: 60 mA
  - Passive Mode: < 6 mA
- Supports Memory Mapped, I/O Mapped, and True IDE Interface Modes
- Supports up to:
    - IDE PIO Mode 6
    - IDE Multi-Word DMA Mode 4
    - IDE Ultra DMA Mode 5
    - PCMCIA Ultra DMA Mode 5
- Hardware RS-code ECC, 4 symbol/page
- Static Wear Leveling
- RoHS compliant
- Optional Industrial Temp Range -40ºC to +85ºC

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1.3 Part Numbering Information

SMART Part Number	Chip Density	Physical Capacity	Sector Card	Head	Cylinder	Sector Track	Un-Formatted Capacity
SG9PC64SME5xxx	**512Mb**	**64MB**	**123,904**	**8**	**484**	**32**	**63,438,848**
SG9PC128SME1xxx	**1Gb**	**128MB**	**248,064**	**8**	**969**	**32**	**127,008,768**
SG9PC256SME1xxx	**1Gb**	**256MB**	**497,152**	**16**	**971**	**32**	**254,541,824**
SG9PC512SME2xxx	**2Gb**	**512MB**	**994,896**	**16**	**987**	**63**	**509,386,752**
SG9PC1GSME4xxx	**4Gb**	**1GB**	**1,989,792**	**16**	**1,974**	**63**	**1,018,773,504**
SG9PC2GSME9xxx	**8Gb**	**2GB**	**3,915,072**	**16**	**3,884**	**63**	**2,004,516,864**
SG9PC4GSMEAxxx	**16Gb**	**4GB**	**7,831,152**	**16**	**7,769**	**63**	**4,009,549,824**
SG9PC8GSMEBxxx	**32Gb**	**8GB**	**15,596,784**	**16**	**15,148**	**63**	**7,985,553,408**
SG9PC16GSMEBxxx	**32Gb**	**16GB**	**31,195,136**	**16**	**16,384**[1]	**63**	**15,971,909,632**
SG9PC32GSMEBxxx	**32Gb**	**32GB**	**61,079,552**	**16**	**16,384**[1]	**63**	**31,272,730,624**

1.4 Part Number Decoder

SG	**9**	**PC**	**xxx**		**SME**	**x**	**x**	**x**	**x**
RoHS-6	Flash Memory	PCMCIA	64: 128: 256: 512: 1G: 2G: 4G: 8G: 16G: 32G:	64MB 128MB 256MB 512MB 1GB 2GB 4GB 8GB 16GB 32GB	Controller SM223	5: 512Mb 1: 1Gb 2: 2Gb 4: 4Gb 9: 8Gb A: 16Gb B: 32Gb	Blank – Commercial I – Industrial	F – Fixed Disk	P – PIO; No DMA

[1] CHS not supported at this capacity

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1.5 Specification Overview

1.5.1 Performance

	Read	Write
▪ Maximum Performance (PIO 6)		
256MB – 16GB	24 MB/s	12 MB/s
128MB	19 MB/s	6 MB/s
64MB	10 MB/s	1.7 MB/s
▪ Maximum Performance (UDMA 4)		
256MB – 16GB	47 MB/s	25 MB/s
128MB	24 MB/s	7 MB/s
64MB	10 MB/s	1.7 MB/s

▪ Host Interface Transfer Rate	16MB/s
▪ Startup Times	
Sleep to Read/Write	<2.5 ms
Power up to Ready	< 100 ms
▪ Command to DRQ	
Read	< 220 us
Write	< 75 us

1.5.2 Reliability

▪ MTBF	> 2,500,000 hours
▪ Data Reliability	1 in 10^{14} bits, read
▪ Data Retention	10 years
▪ Endurance	>2,000,000 program/erase cycles

1.5.3 Power

▪ VCC	5.0V±10%	3.3V±5%
▪ Read	80 mA	60 mA
▪ Write	70 mA	60 mA
▪ Passive	9 mA	6 mA

1.5.4 Environmental

▪ Shock	50G max. @ 11mS
▪ Vibration	15G peak to peak
▪ Operating temperature	0ºC to 70ºC (Commercial) -40ºC to +85ºC (Industrial)
▪ Storage temperature	-65ºC to 150ºC
▪ Humidity	5% to 95%
▪ Altitude	up to 80,000 ft.

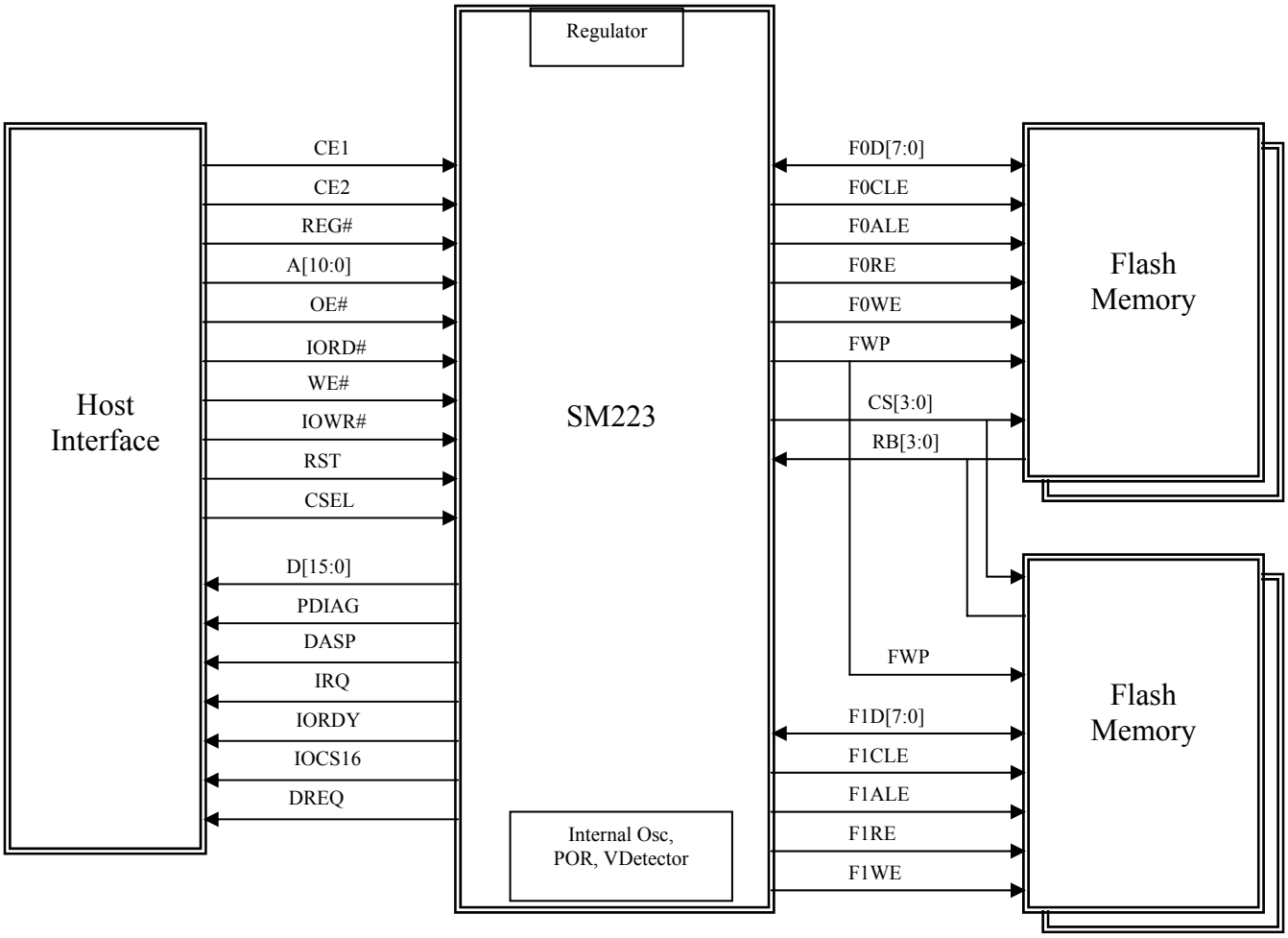
1.5.5 Physical Dimensions

▪ Length	1.433 in. (36.40 mm.)
▪ Width	1.685 in. (42.80 mm.)
▪ Thickness	0.130 in. (3.30 mm.)
▪ Weight	0.36 Oz. (10.2 gm)

2 General Description

The ATA Flash Drive contains a ATA/IDE controller and one or more flash memory devices. The Smart ATA Flash product line is offered in a UL approved Type I housing with a 68 pin PCMCIA connector. On board ATA/IDE controller interfaces with a host system allowing data to be written to and read from the flash memory devices.

2.1 Functional Block Diagram



Notes:
All the signals shown going to the flash devices come from the card controller. All the other signals including those going to the card controller come from the Card Interface.

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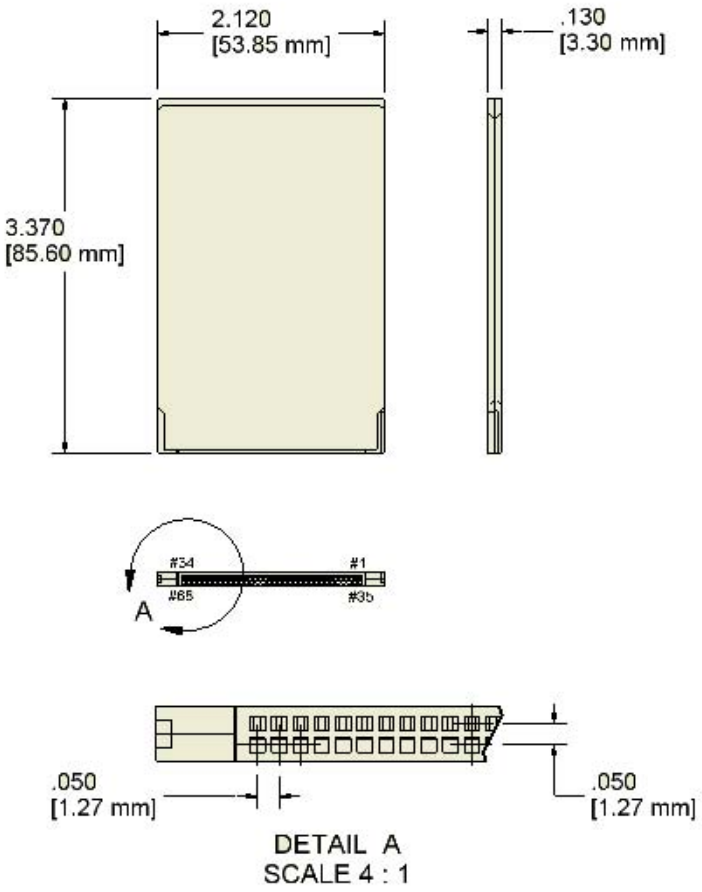
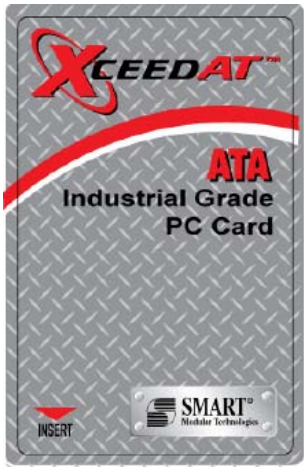
2.2 Mechanical Specifications

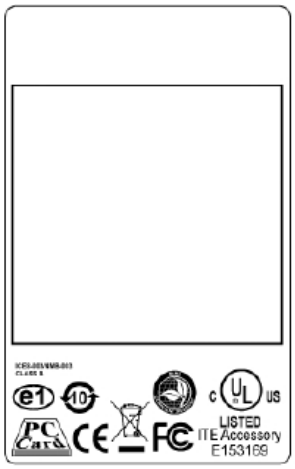


2.3 Labels

Below are images of our standard labels for the ATA Flash card. Part number and manufacturing information are printed on the back of the card.



Front



Back

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3 Electrical Interface

3.1 Electrical Description

The Flash Cards are fully compliant with PCMCIA/ATA specification. This interface standard electrically complies with the PC Card ATA specifications, functioning in I/O Mode, Memory Mode and True IDE Modes.

Table 1 describes the I/O signals. Signals whose source is the host are designated as inputs (I) while signals that the ATA Flash Card sources are outputs (O). Bidirectional signals are designated as Input/Output (I/O). The ATA Flash Drive logic levels conform to those specified in the PCMCIA Release 8 specification. Table 2 describes the signals in the three different operating modes of the card. The three modes are Card Memory, Card I/ O, and True IDE.

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Table 1. Pin Assignments and Pin Type

Card Memory Mode			Card I/O Mode			True IDE Mode		
Pin No.	**Signal Name**	**Pin Type**	**Pin No.**	**Signal Name**	**Pin Type**	**Pin No.**	**Signal Name**	**Pin Type**
1	GND	Ground	1	GND	Ground	1	GND	Ground
2	D3	I/O	2	D3	I/O	2	D3	I/O
3	D4	I/O	3	D4	I/O	3	D4	I/O
4	D5	I/O	4	D5	I/O	4	D5	I/O
5	D6	I/O	5	D6	I/O	5	D6	I/O
6	D7	I/O	6	D7	I/O	6	D7	I/O
7	CE1#	I	7	CE1#	I	7	CS0#	I
8	A10	I	8	A10	I	8	A10	I
9	OE#	I	9	OE#	I	9	OE#	I
10	NC	I	10	A9	I	10	A9	I
11	A9	I	11	A8	I	11	A8	I
12	A8	I	12	A7	I	12	A7	I
13	NC	-	13	VCC	-	13	VCC	-
14	NC	I	14	A6	I	14	A6	I
15	WE#	I		WE#	I		WE#	I
16	RDY/BSY#	O		IREQ#	O		INTRQ	O
17	VCC	Power	51	VCC	Power	51	VCC	Power
18	NC	-	46	NC	-	46	NC	-
19	NC	-	46	NC	-	46	NC	-
20	NC	-	46	NC	-	46	NC	-
21	NC	-	46	NC	-	46	NC	-
22	A7	I		A7	I		A7	I
23	A6	I		A6	I		A6	I
24	A5	I	15	A5	I	15	A5	I
25	A4	I	16	A4	I	16	A4	I
26	A3	I	17	A3	I	17	A3	I
27	A2	I	18	A2	I	18	A2	I
28	A1	I	19	A1	I	19	A1	I
29	A0	I	20	A0	I	20	A0	I
30	D0	I/O	21	D0	I/O	21	D0	I/O
31	D1	I/O	22	D1	I/O	22	D1	I/O
32	D2	I/O	23	D2	I/O	23	D2	I/O
33	WP	O	24	IOIS16#	O	24	IOCS16#	O
34	GND	Ground	35	GND	Ground	35	GND	Ground

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Table 1. Pin Assignments and Pin Type (Continued)

Card Memory Mode			Card I/O Mode			True IDE Mode		
Pin No.	**Signal Name**	**Pin Type**	**Pin No.**	**Signal Name**	**Pin Type**	**Pin No.**	**Signal Name**	**Pin Type**
35	GND	Ground	35	GND	Ground	35	GND	Ground
36	CD1#	O	36	CD1#	O	36	CD1#	O
37	D11	I/O	37	D11	I/O	37	D11	I/O
38	D12	I/O	38	D12	I/O	38	D12	I/O
39	D13	I/O	39	D13	I/O	39	D13	I/O
40	D14	I/O	40	D14	I/O	40	D14	I/O
41	D15	I/O	41	D15	I/O	41	D15	I/O
42	CE2#	I	42	CE2#	I	42	CS1#	I
43	VS1#	O	43	VS1#	O	43	VS1#	O
44	IORD#	I	44	IORD#	I	44	IORD#	I
45	IOWR#	I	45	IOWR#	I	45	IOWR#	I
46	NC	-	46	NC	-	46	NC	-
47	NC	-	47	NC	-	47	NC	-
48	NC	-	48	NC	-	48	NC	-
49	NC	-	49	NC	-	49	NC	-
50	NC	-	50	NC	-	50	NC	-
51	VCC	Power	51	VCC	Power	51	VCC	Power
52	NC	-	52	NC	-	52	NC	-
53	NC	-	53	NC	-	53	NC	-
54	NC	-	54	NC	-	54	NC	-
55	NC	-	55	NC	-	55	NC	-
56	NC	-	56	NC	-	56	CSEL#	I
57	VS2#	O	57	VS2#	O	57	VS2#	O
58	RESET	I	58	RESET	I	58	RESET#	I
59	WAIT#	O	59	WAIT#	O	59	IORDY	O
60	INPACK#	O	60	INPACK#	O	60	DREQ	O
61	REG#	I	61	REG#	I	61	DMACK#	I
62	BVD2	I/O	62	SPKR#	I/O	62	DASP#	I/O
63	BVD1	I/O	63	STSCHG#	I/O	63	PDIAG#	I/O
64	D8	I/O	64	D8	I/O	64	D8	I/O
65	D9	I/O	65	D9	I/O	65	D9	I/O
66	D10	I/O	66	D10	I/O	66	D10	I/O
67	CD2#	O	67	CD2#	O	67	CD2#	O
68	GND	Ground	68	GND	Ground	68	GND	Ground

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Table 2. Signal Description

Signal Name	Mode of Operation	Pin Type	Pin No(s).	Description
CD1#,CD2#		**O**	**36,67**	**Card Detect Outputs**
	Card Memory Mode			These Card Detect pins are connected to ground on the Card. They are used by the host to determine that the Card is fully inserted into the socket.
	Card I/O Mode			This signal is the same in this mode.
	True IDE Mode			This signal is the same in this mode.
IOWR#		**I**	**45**	**I/O Write Input**
	Card Memory Mode			This signal is not used in this mode.
	Card I/O Mode			The I/O Write strobe pulse is used to clock I/O data on the Card data bus into the controller registers. The clocking will occur on the negative to positive going edge of the signal.
	True IDE Mode			This signal has the same function as in Card I/O Mode.
IORD#		**I**	**44**	**I/O Read Input**
	Card Memory Mode			This signal is not used in this mode.
	Card I/O Mode			This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the Card.
	True IDE Mode			This signal has the same function as in Card I/O Mode.
WE#		**I**	**15**	**Write Enable Input**
	Card Memory Mode			This is a signal driven by the host and used for strobing memory write data to the registers of the Card. It is also used for writing the configuration registers
	Card I/O Mode			In this mode, this signal is used to write the CIS and configuration registers
	True IDE Mode			In this mode, this input signal is not used and should be connected to VCC by the host.
CSEL#		**I**	**56**	**Cable Select Input**
	Card Memory Mode			This signal is not used in this mode.
	Card I/O Mode			This signal is not used in this mode.
	True IDE Mode			This signal is used to configure this device as Master or Slave. When this pin is grounded, this device is configured as Master. When this pin is tied to VCC this card is configured as Slave

Table 2. Signal Description (continued)

Signal Name	Mode of Operation	Pin Type	Pin No(s).	Description
OE#		**I**	**9**	**Output Enable Input**
	Card Memory Mode			This is a strobe generated by the host interface. It is used to read data from the Card and to read the CIS and configuration registers
	Card I/O Mode			This signal is used to read the CIS and configuration registers only.
	True IDE Mode			To enable the True IDE Mode, this input should be grounded by the host.
CE1#,CE2# / CS0#, CS1#		**I**	**7,42**	**Card Enable Inputs**
CE1#, CE2#	Card Memory Mode			These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. CE2# always accesses the odd byte of the word. CE1# accesses the even byte or the odd byte of the word depending on A0 and CE2#. A multiplexing scheme based on A0, CE1#, and CE2# allows 8 bit hosts to access all data on D0-D7
	Card I/O Mode			This signal has the same function as in Card Memory Mode.
CS0#, CS1#	True IDE Mode			In the True IDE Mode, CS0# is the chip select for the ATA Command block registers while CS1# is used to select the ATA Control Block registers (Alternate Status Register and the Device Control Registers)
WP/IOIS16# / IOCS16#		**O**	**33**	**Write Protect / I/O Port 16 Output**
WP	Card Memory Mode			The card does not have a WP switch. This signal is held low after reset initialization sequence.
IOIS16#	Card I/O Mode			A low signal indicated that a 16 bit or odd byte only operation can be performed.
IOCS16#	True IDE Mode			This signal is asserted low when the card is expecting a word data transfer cycle. This open collector line is only driven on assertion (low).
GND		**Power**	**1,34,35,68**	**Ground Pin**
VCC		**Power**	**17,51**	**Power Supply Pin**

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Table 2. Signal Description (continued)

Signal Name	Mode of Operation	Pin Type	Pin No(s).	Description
RESET / RESET#		**I**	**58**	**Card Reset Input**
RESET	Card Memory Mode			When this pin is high, this signal resets the Flash Card. The card Reset is only at power-up if this pin is left high or open from power-up. The card is also reset when the Soft Reset bit in the Card Configuration Option Register is set
	Card I/O Mode			This signal has the same function as in Card Memory Mode.
RESET#	True IDE Mode			In this mode, this input pin is active low from the host.
D15-D0		**I/O**	**41,40,39,38,37,66,65,64,6,5,4,3,2,32,31, 30**	**16-bit Data Input/Output Bus**
	Card Memory Mode			These lines carry the Data, Commands, and Status Information between the host and the controller. D15 is the MSB of odd byte and D7 the MSB of even byte in a Word Access.
	Card I/O Mode			This signal has the same function as in Card Memory Mode.
	True IDE Mode			All register operations occur in byte mode on D7-D0, while all data transfers are word (16-bit) accesses.
A10-A0		**I**	**8,11,12,22,23,24,25, 26,27,28, 29**	**Card Address Input Bus**
	Card Memory Mode			These addresses along with the REG# signal are used to select the following: the I/O port address registers in the card, the memory mapped port address registers, a byte in the CIS and Configuration Control and Status registers.
	Card I/O Mode			This signal has the same function as in Card Memory Mode.
A2-A0	True IDE Mode			In this mode, only A2-A0 are used to select one of the Control/Status registers. All the remaining unused address lines should be grounded by the host.

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Table 2. Signal Description (continued)

Signal Name	Mode of Operation	Pin Type	Pin No(s).	Description
REG# / DMACK#		**I**	**61**	**Attribute Memory Select Input / DMA Acknowledge**
REG#	Card Memory Mode			This signal is used to select between Register/ Attribute Memory (REG# = low) and Common Memory (REG# = high)
REG#	Card I/O Mode			Active Low on this signal will allow accesses to I/O space
DMACK#	True IDE Mode			This is the DMA Acknowledge signal that is used for DMA data transfers between host and device. It shall be asserted by the device when it is ready to transfer data to or from the host. This signal is used in a handshake manner with DREQ.
RDY/BSY# / IREQ# / INTRQ		**O**	**16**	**Ready/Interrupt Request Output**
RDY/BSY#	Card Memory Mode			This signal is set high when the card is ready to accept a new data transfer operation and held low when the card is busy. The host must have a pull-up resistor on this signal. When powering-up and when reset, the signal is held low (busy) until the card has completed the power-up or reset operation. When the signal indicates busy no operations to the card are permitted. The signal is held high whenever the card has been powered up with RESET# disconnected or asserted.
IREQ#	Card I/O Mode			In this mode, this signal is used as interrupt request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt. This is set using Configuration Option Register.
INTRQ	True IDE Mode			In this mode, the signal is active high request to the host.
INPACK# / DREQ		**O**	**60**	**Input Port Acknowledge Output / DMA Request**
INPACK#	Card Memory Mode			This signal is not used in this mode.
INPACK#	Card I/O Mode			This signal is asserted by the card when the card is selected and is responding to an I/O read cycle. This signal is used by the host to enable the input data buffers between the host and the card.
DREQ	True IDE Mode			This is the DMA Request that is used for the DMA data transfers between host and device. It shall be asserted by the device when it is ready to transfer data to or from the host. This signal is used in a handshake manner with DMACK#.

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Table 2. Signal Description (continued)

Signal Name	Mode of Operation	Pin Type	Pin No(s).	Description
WAIT# / IORDY		**O**	**59**	**Extend Bus Cycle / I/O Channel Ready Output**
WAIT#	Card Memory Mode			This active low WAIT# Signal is never switched low by the card during Read/Write operations. It is used only at power –up. When both WAIT# and WE# are low at power-on, it forces a boot from the PCMCIA or IDE port rather than from Flash
	Card I/O Mode			This signal has the same function as in Card Memory Mode.
IORDY	True IDE Mode			This signal is held low to extend the host transfer of any host register access (read or write) when the card is not ready to respond to a data transfer request.
BVD1 / STSCHG# / PDIAG#		**O**	**63**	**Battery Voltage Detect Output / Card Status Changed Output / Passed Diagnostics Input/Output**
BVD1	Card Memory Mode			This signal is asserted high since the card does not contain a battery.
STSCHG#	Card I/O Mode			This signal is asserted low to alert the host to changes in the RDY/BSY# and Write Protect states. Its use is controlled through the Card Configuration and Status Registers
PDIAG#	True IDE Mode	I/O		This signal is asserted by slave drive to indicate to master drive that it has completed diagnostics and is ready to provide status.
BVD2 / SPKR# / DASP#		**O**	**62**	**Battery Voltage Detect Output / Audio Waveform Output / Drive Active/Drive 1 Preset Output**
BVD2	Card Memory Mode			This signal is asserted high since the card does not contain a battery
SPKR#	Card I/O Mode			This signal is asserted high since the card does not support audio.
DASP#	True IDE Mode	I/O		This signal indicates that a drive is active or that a slave drive (Drive 1) is present.
VS1#, VS2#		**O**	**43,57**	**Voltage Sense Outputs**
	Card Memory Mode			VS1# is grounded so that the Card's CIS can be read at 3.3V and VS2# is left open.
	Card I/O Mode			This signal is the same in this mode.
	True IDE Mode			This signal is the same in this mode.

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Table 3. Host Signal Termination

Item	Signal	Host
Status Signal	**RDY/BSY#** **WAIT#** **WP**	Pull-up to Vcc R ≥ 10 KΩ
	INPACK#	In PCMCIA modes Pull-up to Vcc R ≥ 10 KΩ In True IDE mode, if DMA operation is supported by the host, Pull-down to GND R ≥ 5.6 KΩ PCMCIA / True IDE hosts switch the pull-up to pull-down in IDE mode if DMA operation is supported. The PCMCIA mode Pull-up may be left active during True IDE mode if True IDE DMA operation is not supported.
Voltage Sense	**VS1** **VS2**	Pull up to VCC 10 KΩ ≤ R ≤ 100 KΩ
Battery/Detect	**BVD[2:1]**	Pull-up R ≥ 50 KΩ

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3.2 Card Configuration

3.2.1 Registers and Memory Space Decoding

CE2#	CE1#	REG#	OE#	WE#	A10	A9	A8-A4	A3	A2	A1	A0	Selected Space
1	1	X	X	X	X	X	XX	X	X	X	X	Standby
X	0	0	0	1	X	1	XX	X	X	X	0	Configuration Register Read
1	0	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8 bit – D7-D0)
0	1	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8 bit – D15-D8)
0	0	1	0	1	X	X	XX	X	X	X	0	Common Memory Read (16 bit – D15-D0)
X	0	0	1	0	X	1	XX	X	X	X	0	Configuration Register Write
1	0	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8 bit – D7-D0)
0	1	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8 bit – D7-D0)
0	0	1	1	0	X	X	XX	X	X	X	0	Common Memory Write (8 bit – D7-D0)
X	0	0	0	1	0	0	XX	X	X	X	0	Card Information Structure Read
1	0	0	1	0	0	0	XX	X	X	X	0	Invalid Access (CIS Write)
1	0	0	0	1	X	X	XX	X	X	X	1	Invalid Access (Odd Attribute Read)
1	0	0	1	0	X	X	XX	X	X	X	1	Invalid Access (Odd Attribute Write)
0	1	0	0	1	X	X	XX	X	X	X	X	Invalid Access (Odd Attribute Read)
0	1	0	1	0	X	X	XX	X	X	X	X	Invalid Access (Odd Attribute Write)

3.2.2 Configuration Registers Decoding

CE2#	CE1#	REG#	OE#	WE#	A10	A9	A8-A4	A3	A2	A1	A0	Selected Space
X	0	0	0	1	0	1	00	0	0	0	0	Configuration Option Register Read (200h)
X	0	0	1	0	0	1	00	0	0	0	0	Configuration Option Register Write (200h)
X	0	0	0	1	0	1	00	0	0	1	0	Card Status Register Read (202h)
X	0	0	1	0	0	1	00	0	0	1	0	Card Status Register Write (202h)
X	0	0	0	1	0	1	00	0	1	0	0	Pin Replacement Register Read (204h)
X	0	0	1	0	0	1	00	0	1	0	0	Pin Replacement Register Write (204h)
X	0	0	0	1	0	1	00	0	1	1	0	Socket and Copy Register Read (206h)
X	0	0	1	0	0	1	00	0	1	1	0	Socket and Copy Register Write (206h)

Note: The location of the Card Configuration Registers should always be read from the CIS since these locations may vary in future products. No Writes should be performed to the Card Attribute Memory except to the Card Configuration Register Addresses. All other attribute memory locations are reserved.

3.3 Configuration Register Description

3.3.1 Configuration Option Register (Address 200h in attribute memory)

The configuration Option Register is used to configure the card's interface, address decoding and interrupt and to issue a soft reset to the PC Card. This register is reset at System Power-On and by the RESET signal (after the flash card is configured in PC Card or ATA extension mode).

Operation	B7	B6	B5	B4	B3	B2	B1	B0
R/W	SRESET	LevlREQ	CONF5	CONF4	CONF3	CONF2	CONF1	CONF0

SRESET — When this bit is set to logic one, the Host interface is in the reset state. This reset conditions is the same as a hardware or power-on reset state with the exception that this bit stays set, and the configuration as PCMCIA remains set. This software reset condition is removed when this bit is reset to logic zero. Following a power-on or hardware reset, this bit is cleared.

LevlREQ — This bit is set to one for level mode interrupt and set to zero for pulse mode interrupt. In pulse mode interrupt, the pulse width is at least 0.5uS. In level mode interrupt, the interrupt line is low state until the interrupt is serviced by the system. The interrupt is driven in the inactive state.

CONF5-CONF0 — Configuration Index. Set to zero by reset. It's used to select operation mode of the Card as shown below. Please note that CONF5 and CONF4 are reserved and must be written as zero. See the table below.

CONF5	CONF4	CONF3	CONF2	CONF1	CONF0	Card Mode
0	0	0	0	0	0	Memory Mapped
0	0	0	0	0	1	I/O Mapped, 16 contiguous registers
0	0	0	0	1	0	Primary I/O Mapped, 1F0-1F7/3F6-3F7
0	0	0	0	1	1	Secondary I/O Mapped, 170-177/376-377

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3.3.2 Card Status Register (Address 202h in attribute memory)

This register contains information about the card's condition.

Operation	B7	B6	B5	B4	B3	B2	B1	B0
Read	Changed	SigChg	IOIs8	0	0	PwrDwn	Int	0
Write	0	SigChg	IOIs8	0	0	PwrDwn	0	0

Changed	Indicates that one or both of the Pin Replacement Register CRdy, or CWProt bits are set to one.
SigChg	This field serves as a gate for the STSCHG# signal. When the card is configured as I/O interface, and if this and the Changed field are set to one, the function shall assert STSCHG#. If this field is reset to zero, the card shall not assert STSCHG#.
IOIs8	The host sets this bit to a one if the Card is to be configured in an 8 bit I/O mode. The control for an 8-bit data access is built into the ATA command set, and still must be used.
PwrDwn	When the host sets this field to one, the card shall enter a power-down state. When this field is one, the host shall not access the card. The host shall return this field to zero before attempting to access the function. The host can set this function only if the card indicates it is ready. The RDY/BSY# value becomes busy when this bit is changed. RDY/BSY# will not become ready until the power state requested has been entered. The Card automatically powers down when it is idle and powers back up when it receives a command.
Int	This bit represents the internal state of the interrupt request. This value is available whether or not I/O interface has been configured. This signal remains true until the condition which caused the interrupt request has been serviced. If interrupts are disabled by the IEN# bit in the device control register, this bit is a zero.

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3.3.3 Pin Replacement Register (Address 204h in attribute memory)

This register provides status for signals on the CF Card interface that are used in Memory Access Mode but assume a different meaning or use in I/O Mode. The register may be read and written; however, when written, the lower four bits act as a mask for changing the corresponding upper four bits.

Operation	B7	B6	B5	B4	B3	B2	B1	B0
Read	0	0	Crdy/Bsy#	CWProt	0	0	Mrdy/Bsy	MWProt
Write	0	0	Crdy/Bsy#	CWProt	0	0	Mrdy/Bsy	MWProt

CRdy/Bsy#	This bit is set to one when the bit RRdy/Bsy# changes state. This bit must be cleared by the host.
CWProt	This bit is set to one when the RWprot changes state.This bit must be cleared by the host.
RRdy/Bsy#	When read this bit represents the internal state of the RDY/BSY# signal. This bit may be used to read the state of RDY/BSY# as that pin has been reallocated to use as Interrupt Request when the card is configured as I/O interface.
RWProt	This bit is always zero, since the card does not support a WP switch.
MRdy/Bsy#	This bit acts as a mask for writing the corresponding CRdy/Bsy# bit.
MWProt	This bit acts as a mask for writing the corresponding CWprot bit.

Initial value of "C" bit	Written by Host		Final value of "C" bit	Comment
	"C" Bit	"M" Bit		
0	X	0	0	Unchanged
1	X	0	1	Unchanged
X	0	1	0	Cleared by host
X	1	1	1	Set by host

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3.3.4 Socket and Copy Register (Address 206h in attribute memory)

This register contains additional configuration information. This register may be used by the host system to implement a substitute for the ATA Master/Slave functionality. This register is always written by the system before writing the card's Configuration Index register.

Operation	B7	B6	B5	B4	B3	B2	B1	B0
Read	Reserved	Copy Number			Socket Number			
Write	0	Copy Number			Socket Number			

Reserved	This bit is reserved for future standardization. This bit must be set to zero by the software when the register is written.
Copy Number	Drive's which indicate in their CIS that they support more than one copy of identically configured drive-cards, should have a copy number in this field. Only 0 or 1 is allowed
Socket Number	This field indicates to the Flash Drive that it is located in the nth socket. The first socket is numbered 0.

3.4 Truth Tables (Transfer function tables)

3.4.1 Attribute Memory Table

REG#	CE2#	CE1#	A9	A0	OE#	WE#	D15-D8	D7-D0	Function Mode
X	1	1	X	X	X	X	High Z	High Z	Standby
0	1	0	0	0	0	1	High Z	Data	Read CIS (8 bits)
0	1	0	0	0	1	0	XX	Data	Write CIS (8 bits)
0	1	0	1	0	0	1	High Z	Data	Read Configuration Registers (8 bits)
0	1	0	1	0	1	0	XX	Data	Read Configuration Registers (8 bits)
0	0	0	0	X	0	1	Invalid	Data	Read CIS (16 bits)
0	0	0	0	X	1	0	XX	Data	Write CIS (16 bits)
0	0	0	1	X	0	1	Invalid	Data	Read Configuration Registers (16 bits)
0	0	0	1	X	1	0	XX	Data	Read Configuration Registers (16 bits)

Note: The CE# signal or both the OE# signal and the WE# signal must be de-asserted between consecutive cycle operations.

3.4.2 Common Memory Table

The common memory accesses can be either 8 bit or 16 bit. The Card permits both 8 and 16 bit accesses to all of its common memory addresses.
The Card may request the host to extend the length of a memory write cycle or extend the length of a memory read cycle until data is ready by asserting the WAIT# signal at the start of the cycle.

REG#	CE2#	CE1#	A0	OE#	WE#	D15-D8	D7-D0	Function Mode
X	1	1	X	X	X	High Z	High Z	Standby Mode
1	1	0	0	0	1	High Z	Even Byte	Byte Read (8 bits)
1	1	0	1	0	1	High Z	Odd Byte	
1	1	0	0	1	0	XX	Even Byte	Byte Write (8 bits)
1	1	0	1	1	0	XX	Odd Byte	
1	0	0	X	0	1	Odd Byte	Even Byte	Word Read (16 bits)
1	0	0	X	1	0	Odd Byte	Even Byte	Word Write (16 bits)
1	0	1	X	0	1	Odd Byte	High Z	Odd Byte Read (8 bits)
1	0	1	X	1	0	Odd Byte	XX	Odd Byte Write (8 bits)

3.4.3 I/O Interface Table

The I/O accesses can be either 8 bit or 16 bit. when a 16 bit port is addressed the signal IOIS16# is asserted by the PC card. Otherwise this signal is de-asserted. If on the other hand, when a 16-bit transfer is attempted and this signal is not asserted, the host must generate a pair of 8-bit references to access the even and odd bytes.
The Card may request the host to extend the length of a memory write cycle or extend the length of a memory read cycle until data is ready by asserting the WAIT# signal at the start of the cycle.

REG#	CE2#	CE1#	A0	IORD#	IOWR#	D15-D8	D7-D0	Function Mode
X	1	1	X	X	X	High Z	High Z	Standby Mode
0	1	0	0	0	1	High Z	Even Byte	Byte Input Access (8 bits)
0	1	0	1	0	1	High Z	Odd Byte	
0	1	0	0	1	0	XX	Even Byte	Byte Output Access (8 bits)
0	1	0	1	1	0	XX	Odd Byte	
0	0	0	0	0	1	Odd Byte	Even Byte	Word Input Access (8 bit)
0	0	0	0	1	0	Odd Byte	Even Byte	Word Output Access (8 bit)
1	X	X	X	0	1	XX	XX	I/O Read Inhibit
1	X	X	X	1	0	High Z	High Z	I/O Write Inhibit
0	0	1	X	0	1	Odd Byte	High Z	Odd Byte Input only (8 bits)
0	0	1	X	1	0	Odd Byte	XX	Odd Byte Output only (8 bits)

3.4.4 True IDE Mode Table

The Card can be configured in a True IDE Mode of operation. The Card can be configured in this mode only when the OE# signal is grounded by the host during the power off to power on cycle. In this True IDE Mode the Card protocol and configuration are disabled and only I/O operations to the task file and Data Registers are allowed. In this mode no memory or attribute registers are accessible to the host.

Removing PCMCIA Card and re-inserting the card while the host is powered-on will reconfigure the card into ATA mode from the original True IDE mode. To configure the card in the True IDE mode, the socket must be powered cycled with the Card inserted and the OE# asserted.

CS1#	CS0#	A2-A0	IORD#	IOWR#	D15-D8	D7-D0	Function Mode
0	0	X	X	X	High Z	High Z	Invalid
1	1	X	X	X	High Z	High Z	Standby Mode
1	0	1-7h	1	0	XX	Data In	Task File Write
1	0	1-7h	0	1	High Z	Data Out	Task File Read
1	0	0	1	0	Odd Byte in	Even Byte in	Data Register Write
1	0	0	0	1	Odd Byte out	Even Byte out	Data Register Read
0	1	6h	1	0	XX	Control In	Control Register Write
0	1	6h	0	1	High Z	Status Out	All Status Read

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3.5 ATA Specific Register Mapping

The Card can be configured as a high performance I/O device through

a. Standard PC-AT disk I/O address spaces 1F0h~1F7h, 3F6h~3F7h (primary), 170h~177h, 376h~377h (secondary) with IRQ14 (or other available IRQ).
b. Any system decoded 16 byte I/O block using any available IRQ.
c. Memory Space.

The communication to or from the Card is done using the Task File registers which provide all the necessary registers for control and status information. The Card interface connects peripherals to the host using four register mapping methods.The following is a detailed description of these methods:

Standard Configurations				
Config Index	**I/O or Memory**	**Address**	**Drive#**	**Description**
0 & 8	Memory	0-Fh, 400-7FFh	0	Memory Mapped
1 & 9	I/O	Xx0-xxFh	0	I/O Mapped 16 contiguous registers
2 & Ah	I/O	1F0h-1F7h, 3F6h-3F7h	0	Primary I/O Mapped Drive 0
2 & Ah	I/O	1F0h-1F7h, 3F6h-3F7h	1	Primary I/O Mapped Drive 1
3 & Bh	I/O	1F0h-1F7h, 3F6h-3F7h	0	Secondary I/O Mapped Drive 0
3 & Bh	I/O	1F0h-1F7h, 3F6h-3F7h	1	Secondary I/O Mapped Drive 1

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3.5.1 Memory Mapped Addressing

When the Card registers are accessed via memory references, the registers appear in the common memory space window: 0~2K bytes as follows:

REG#	A10	A9-A4	A3	A2	A1	A0	Offset	OE# = 0	WE# = 0	Notes
1	0	X	0	0	0	0	0	Even RD Data	Even WR Data	1
1	0	X	0	0	0	1	1	Error	Features	2
1	0	X	0	0	1	0	2	Sector Count	Sector Count	
1	0	X	0	0	1	1	3	Sector No.	Sector No.	
1	0	X	0	1	0	0	4	Cylinder Low	Cylinder Low	
1	0	X	0	1	0	1	5	Cylinder High	Cylinder High	
1	0	X	0	1	1	0	6	Select Card/Head	Select Card/Head	
1	0	X	0	1	1	1	7	Status	Command	
1	0	X	1	0	0	0	8	Duplicate Even RD Data	Duplicate Even WR Data	2
1	0	X	1	0	0	1	9	Duplicate Odd RD Data	Duplicate Odd WR Data	2
1	0	X	1	1	0	1	D	Duplicate Error	Duplicate Feature	2
1	0	X	1	1	1	0	E	Alternate Status	Device Control	
1	0	X	1	1	1	1	F	Drive Address	Reserved	
1	1	X	X	X	X	0	8	Even RD Data	Even WR Data	3
1	1	X	X	X	X	1	9	Odd RD Data	Odd WR Data	3

Notes:

1. Register 0 is accessed with CE1# and CE2# low as a word register on the combined odd data bus and even data bus. This register may also be accessed by a pair of byte accesses to the offset 0 with CE1# low and CE2# high. Note that the address space of this word register overlaps the address space of the Error/Feature byte-wide registers that lie at offset 1. When accessed twice at byte register with CE1# low, the first to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access. A byte access to register 0 with CE1# high and CE2# low accesses the error (when read) or feature (when written) register.
2. Register at offset 8, 9 and D are non-overlapping duplicates of the registers at offset 0 and 1. Therefore, if the registers are byte accessed in the order 9 and then 8 the data will be transferred odd byte then even byte. Repeated byte accesses to register 8 or 0 will access consecutive (even then odd) bytes from the data buffer. Repeated word accesses to register 8, 9, or 0 will access consecutive words from the data buffer. Repeated byte accesses to register 9 are not supported. However, repeated alternating byte accesses to registers 8 then 9 will access consecutive (even then odd) bytes from the data buffer. Byte accesses to register 9 access only the odd byte of the data.
3. Accesses to even addresses between 400h and 7FFh access register 8. Accesses to odd addresses between 400h and 7FFh access register 9. This 1K byte memory window to the data register is provided so that hosts can perform memory to memory block moves to the data register when the register lies in memory space. Some hosts, such as the X86 processors, must increment both the source and destination addresses when executing the memory to memory block move instruction. Some Card adapters also have auto incrementing logic embedded within them. This address window allows these hosts and adapters to function efficiently. Note that this entire window accesses the Date Register FIFO and does not allow random access to the data buffer within the PC Card.

3.5.2 Contiguous I/O Mapped Addressing

When the system decodes a contiguous block of I/O registers to select the CF Card, the registers are accessed in the block of I/O space decoded by the system as follows:

REG#	A3	A2	A1	A0	Offset	IORD# = 0	IOWR# = 0	Notes
1	0	0	0	0	0	Even RD Data	Even WR Data	1
1	0	0	0	1	1	Error	Features	2
1	0	0	1	0	2	Sector Count	Sector Count	
1	0	0	1	1	3	Sector No.	Sector No.	
1	0	1	0	0	4	Cylinder Low	Cylinder Low	
1	0	1	0	1	5	Cylinder High	Cylinder High	
1	0	1	1	0	6	Select Card/Head	Select Card/Head	
1	0	1	1	1	7	Status	Command	
1	1	0	0	0	8	Duplicate Even RD Data	Duplicate Even WR Data	2
1	1	0	0	1	9	Duplicate Odd RD Data	Duplicate Odd WR Data	2
1	1	1	0	1	D	Duplicate Error	Duplicate Feature	2
1	1	1	1	0	E	Alternate Status	Device Control	
1	1	1	1	1	F	Drive Address	Reserved	

Notes:
1. Register 0 is accessed with CE1# and CE2# low as a word register on the combined odd data bus and even data bus. This register may also be accessed by a pair of byte accesses to the offset 0 with CE1# low and CE2# high. Note that the address space of this word register overlaps the address space of the Error/Feature byte-wide registers that lie at offset 1. When accessed twice at byte register with CE1# low, the first to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access. A byte access to register 0 with CE1# high and CE2# low accesses the error (when read) or feature (when written) register.
2. Register at offset 8, 9 and D are non-overlapping duplicates of the registers at offset 0 and 1. Therefore, if the registers are byte accessed in the order 9 and then 8 the data will be transferred odd byte then even byte. Repeated byte accesses to register 8 or 0 will access consecutive (even then odd) bytes from the data buffer. Repeated word accesses to register 8, 9, or 0 will access consecutive words from the data buffer. Repeated byte accesses to register 9 are not supported. However, repeated alternating byte accesses to registers 8 then 9 will access consecutive (even then odd) bytes from the data buffer. Byte accesses to register 9 access only the odd byte of the data.
3. Address lines not indicated, are ignored by the Card for accessing all the registers in this table.

3.5.3 I/O Primary and Secondary Addressing

REG#	A9-A4	A3	A2	A1	A0	IORD# = 0	IOWR# = 0	Notes
0	1F(17)h	0	0	0	0	Even RD Data	Even WR Data	1,2
0	1F(17)h	0	0	0	1	Error	Features	2
0	1F(17)h	0	0	1	0	Sector Count	Sector Count	
0	1F(17)h	0	0	1	1	Sector No.	Sector No.	
0	1F(17)h	0	1	0	0	Cylinder Low	Cylinder Low	
0	1F(17)h	0	1	0	1	Cylinder High	Cylinder High	
0	1F(17)h	0	1	1	0	Select Card/Head	Select Card/Head	
0	1F(17)h	0	1	1	1	Status	Command	
0	3F(37)h	0	1	1	0	Alternate Status	Device Control	
0	3F(37)h	0	1	1	1	Drive Address	Reserved	

Notes:
1. Register 0 is accessed with CE1# and CE2# low as a word register on the combined odd data bus and even data bus. This register may also be accessed by a pair of byte accesses to the offset 0 with CE1# low and CE2# high. Note that the address space of this word register overlaps the address space of the Error/Feature byte-wide registers that lie at offset 1. When accessed twice at byte register with CE1# low, the first to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access.
2. A byte access to register 0 with CE1# high and CE2# low accesses the error (when read) or feature (when written) register.
3. Address lines which are not indicated are ignored by the Card for accessing all the registers in this table.

3.5.4 True IDE Mode Addressing

When the Card is configured in the True IDE mode, the I/O decoding is as follows:

CS1#	CS0#	A2	A1	A0	IORD# = 0	IOWR# = 0
1	0	0	0	0	Even RD Data	Even WR Data
1	0	0	0	1	Error	Features
1	0	0	1	0	Sector Count	Sector Count
1	0	0	1	1	Sector No.	Sector No.
1	0	1	0	0	Cylinder Low	Cylinder Low
1	0	1	0	1	Cylinder High	Cylinder High
1	0	1	1	0	Select Card/Head	Select Card/Head
1	0	1	1	1	Status	Command
0	1	1	1	0	Alternate Status	Device Control
0	1	1	1	1	Drive Address	Reserved

3.6 ATA Registers (Task File Registers)

The following section describes the hardware registers used by the host software to issue commands to the CF Card. These registers are often collectively referred to as the "Task File" registers.

Note: In accordance with the Card specifications, each of the registers which is located at an odd offset address may be accessed at its normal address and also the corresponding even address (normal address -1) using data bus lines (D15~D8) when CE1# is high and CE2# is low unless IOIS16# is high (not asserted) and I/O cycle is being performed.

3.6.1 Data Register (Address – 1F0/170; offset – 0, 8, 9)

CE2#	CE1#	A0	Offset	Data Bus	Data Register
0	0	X	0, 8, 9	D15-D0	Word Data Register
1	0	0	0, 8	D7-D0	Even Data Register
1	0	1	9	D7-D0	Odd Data Register
0	1	X	8, 9	D15-D8	Odd Data Register
1	0	1	1, D	D7-D0	Error/Feature Register
0	1	X	1	D15-D8	Error/Feature Register
0	0	X	D	D15-D8	Error/Feature Register

The data register is a 16 bit register and it used to transfer data blocks between the Card data buffer and the host. This register overlaps the Error register.

The table above describes the combinations of data register access and is provided to assist in understanding the overlapped Data Register and Error/Feature Register rather than to attempt to define general Word and byte access modes and operations. See section 3.4 for various function transfer tables.

Note: Because of the overlapped register, access to the 1F1h and 171h or offset 1 are not defined for word (CE2# = 0 and CE1# = 0) operations. These accesses are treated as accesses to the Word Data Register. The duplicated registers at offsets 8h, 9h, Dh have no restrictions on the operations that can be performed by the socket.

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3.6.2 Error Register (Address – 1F1/171; offset – 1, Dh; Read Only)

This register contains additional information about the source of an error when an error is indicated in bit 0 of the Status Register. The bits are defined as follows:

B7	B6	B5	B4	B3	B2	B1	B0
BBK	UNC	0	IDNF	0	ABRT	0	AMNF

This register is also accessed on data bits D15-D8 during a write operation to offset 0 with CE2# low and CE1# high.

Bit 7 (BBK) This bit is set when a Bad Block is detected. This bit is set when Error on Drive 1 (True IDE).

Bit 6 (UNC) This bit is set when an Uncorrectable Read Error is encountered.

Bit 5 This bit is set to 0.

Bit 4 (IDNF) The requested sector ID is in error or cannot be found.

Bit 3 This bit is set to 0.

Bit 2 (ABRT) This bit is set if the command has been aborted because card status: Not Ready, Write Fault, or when an invalid command has been issued.

Bit 1 This bit is set to 0.

Bit 0 (AMNF) This bit is set in case of a general error.

3.6.3 Feature Register (Address - 1F1/171; offset - 1, Dh; Write Only)

This register provides information regarding features of the Card that the host can utilize. This register is also accessed on data bits D15~D8 during a write operation to offset 0 with CE2# low and CE1# high.

3.6.4 Sector Count Register (Address - 1F2/172; offset - 2)

This register contains the number of sector.s of data requested to be transferred on a read or write operation between the host and the PC Card. If the value in this register is zero, a count of 256 sectors is specified. If the command was successful, this register is zero at command completion. If not successfully completed, the register contains the number of sectors that need to be transferred to complete the request.

3.6.5 Sector Number (LBA 7~0) Register (Address - 1F3/173; offset - 3)

This register contains starting sector number or bits 7~0 of the Logical Block Address (LBA) for any Card data access for the subsequent command.

3.6.6 Cylinder Low (LBA 15~8) Register (Address - 1F4/174; offset - 4)

This register contains the low order 8 bits of the starting cylinder address or bits15~8 of the Logical Block Address (LBA).

3.6.7 Cylinder High (LBA 23~16) Register (Address - 1F5/175; offset - 5)

This register contains the high order 8 bits of the starting cylinder address or bits 23~16 of the Logical Block Address (LBA).

3.6.8 Drive/Head (LBA 27~24) Register (Address - 1F6/176; offset - 6)

The Drive/Head register is used to select the drive and head. It is also used to select the LBA addressing instead of cylinder/ head/sector addressing. The bits are defined as follows:

B7	B6	B5	B4	B3	B2	B1	B0
1	LBA	1	DRV	HS3	HS2	HS1	HS0

This register is also accessed on data bits D15-D8 during a write operation to offset 0 with CE2# low and CE1# high.

Bit 7 — This bit is set to 1.

Bit 6 (LBA) — LBA is a flag to select either cylinder/head/sector (CHS) or LBA Mode. When this bit is zero, CHS mode is selected. When this bit is one, LBA mode is selected. In LBA Mode, the LBA is interpreted as follows:
LBA7~LBA0: Sector Number Register D7~D0
LBA15~LBA8: Cylinder Low Register D7~D0
LBA23~LBA16: Cylinder High Register D7~D0
LBA27~LBA24: Drive/Head Register HS3~HS0

Bit 5 — This bit is set to 1.

Bit 4 (DRV) — DRV is the drive number. When DRV is zero, drive/card 0 is selected. When DRV is one, drive/card 1 is selected. The Card is set to be card 0 or 1 using the copy field (Drive#) of the Card Socket & Copy configuration register.

Bit 3 (HS3) — When operating in the CHS mode, this is bit 3 of the head number. It is Bit 27 when in LBA mode.

Bit 2 (HS2) — When operating in the CHS mode, this is bit 2 of the head number. It is Bit 26 when in LBA mode.

Bit 1 (HS1) — When operating in the CHS mode, this is bit 1 of the head number. It is Bit 25 when in LBA mode.

Bit 0 (HS0) — When operating in the CHS mode, this is bit 0 of the head number. It is Bit 24 when in LBA mode.

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3.6.9 Status & Alternate Status Register (Address - 1F7/177 & 3F6/376; offset - 7, Eh; Read only)

This register returns the Card status when read by the host. Reading the status register does clear a pending interrupt while reading the alternate status register does not. The status and alternate status registers are read only registers. When writing to the address of the status register command register is written. When writing to the address of the alternate status register, device control register is written. The status bits are defined as follows:

B7	B6	B5	B4	B3	B2	B1	B0
BUSY	RDY	DWF	DSC	DRQ	CORR	0	ERR

Bit 7 (BUSY) When the busy bit is set, the controller is executing a command. Also, when this bit is set, the host may not read or write any other register except the Status, Alternate Status, Device Control, or Drive Address registers. This bit is set when RESET# is asserted. It is also set when an AT host sets Device Control Register, Bit 2 or when the Command registers is loaded by the host.

Bit 6 (RDY) RDY indicated whether the device is capable of performing Card operations. This bit is cleared at power up and remains cleared until the Card is ready to accept a command.

Bit 5 (DWF) This bit, if set, indicates a write fault has occurred.

Bit 4 (DSC) This bit is set when the Card is ready. This bit is cleared at power up.

Bit 3 (DRQ) The bit is set when the Card requires that information be transferred either to or from the host through the data register.

Bit 2 (CORR) This bit is set when a correctable data error has been encountered and the data has been corrected. This condition does not terminate a multi-sector read operation. This bit is cleared when the Command register is written.

Bit 1 This bit is always set to 0.

Bit 0 (ERR) This bit is set when the previous command has ended in some type of error. The bits in the error register contain additional information describing the error. This bit is cleared when the Command register is written.

3.6.10 Command Register (Address - 1F7/177; offset - 7; Write only)

The Command register contains the command code being sent to the device. Command execution begins immediately after this register is written.The Command register is a write only register. When reading from the address of the Command register, the Status register is read.

3.6.11 Device Control Register (Address - 3F6/376; offset - Eh; Write only)

This register is used to control the Card interrupt request and to issue an ATA soft reset to the card. This register can be written even if the card is BUSY. The bits are defined as follows:

B7	B6	B5	B4	B3	B2	B1	B0
X	X	X	X	HD3En	SW Rst	IEn#	0

Bit 7 – Bit 4 — These bits are don't care. But it is recommended that the user program these bits to zero.

Bit 3 (HD3En) — This bit is set to enable bit 3 of the address of the selected drive head giving a 4-bit addressable range corresponding to 1 to 16 heads.

Bit 2 (SW Rst) — This bit is set to one in order to force the Card to perform an AT Disk controller soft reset operation. This does not change the Card configuration registers as hardware reset does. The card remains in reset until this bit is reset to zero.

Bit 1 (IEn#) — The interrupt enable bit enables interrupts when the bit is zero. When this bit is set to one, interrupts from the Card are disabled. This bit also controls the Int bit in the configuration and status register. This bit is set to one at power on and reset.

Bit 0 — This bit is ignored by the PCMCIA storage card

3.6.12 Drive Address Register (Address - 3F7/377; offset - Fh; Read only)

This is a diagnostic loop back register that contains Write Gate, Head Select3/Reduced Write Current, Head Select 2, Head Select 1, Head Select 0, Drive Select Drive 1, and Drive Select Drive 0. These bits reflect the state of the signals on the control cable. The host may read this register at any time. When host reads this register, only bits 6:0 are driven, bit 7 is High Impedance. NOTE: The Drive Address Register, also referred to as the Digital Input Register, is no longer supported in the ATA specifications. However, for backward compatibility, the PCMCIA Cards still supports this register, and responds as described.

B7	B6	B5	B4	B3	B2	B1	B0
HiZ	Wgate	H3/RWC	H2	H1	H0	DS1	DS0

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4 ATA Command Description

This section documents the Host Interface Commands supported by the Flash Card Controller. Two standard classes of interface specifications are currently implemented: the AT Attachment interface specifications, and the CFA PCMCIA Specifications. In additions, this card conforms with the PC Card specifications when operating in the PC Card Mode and the ATA specifications when operating in the true IDE mode.

Each command is discussed in terms of the contents of the Task File when the command is issued, the contents of the Task File when the host read the status after the command is completed, as well as the data that is transferred in response to the command issued.

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4.1 ATA Command Set

The table below summarizes the ATA command set with the paragraphs that follow describing the individual commands and the task file for each.

Class	Command	Code	FR	SC	SN	CY	DR	HD	LBA
1	Check Power Mode	E5h or 98h	-	-	-	-	V	-	-
1	Execute Drive Diagnostic	90h	-	-	-	-	-	-	-
1	Erase Sector(s)	C0h	-	V	V	V	V	V	V
2	Format Track	50h	-	V	-	V	V	V	V
1	Identify Device	ECh	-	-	-	-	V	-	-
1	Idle	E3h or 97h	-	V	-	-	V	-	-
1	Idle Immediate	E1h or 95h	-	-	-	-	V	-	-
1	Initialize Drive Parameters	91h	-	V	-	-	V	V	-
1	Read Buffer	E4h	-	-	-	-	V	-	-
1	Read DMA	C8h	-	V	V	V	V	V	V
1	Read Multiple	C4h	-	V	V	V	V	V	V
1	Read Sector(s)	20h or 21h	-	V	V	V	V	V	V
1	Read Verify Sector(s)	40h or 41h	-	V	V	V	V	V	V
1	Recalibrate	1Xh	-	-	-	-	V	-	-
1	Request Sense	03h	-	-	-	-	V	-	-
1	Seek	7Xh	-	-	V	V	V	V	V
1	Set Features	EFh	V	-	-	-	V	-	-
1	Set Multiple Mode	C6h	-	V	-	-	V	-	-
1	Set Sleep Mode	E6h or 99h	-	-	-	-	V	-	-
1	Stand By	E2h or 96h	-	-	-	-	V	-	-
1	Stand By Immediate	E0h or 94h	-	-	-	-	V	-	-
1	Translate Sector	87h	-	V	V	V	V	V	V
1	Wear Level	F5h	-	-	-	-	V	V	-
2	Write Buffer	E8h	-	-	-	-	V	-	-
2	Write DMA	CAh	-	V	V	V	V	V	V
3	Write Multiple	C5h	-	V	V	V	V	V	V
3	Write Multiple w/o Erase	CDh	-	V	V	V	V	V	V
2	Write Sectors(s)	30h or 31h	-	V	V	V	V	V	V
2	Write Sector(s) w/o Erase	38h	-	V	V	V	V	V	V
3	Write Verify	3Ch	-	V	V	V	V	V	V

Notes:

1. Register Abbreviation:

FR - Feature Register
SC - Sector Count Register
SN: - Sector Number Register
CY - Cylinder Low/High Register
DR - Drive bit of Drive/Head Register
HD - Head No. (0 to 15) of Drive/Head Register

V*: used for the command*

1. - : *not used for the command*

4.2 ATA Command Set Definition

This section details the functionality of commands supported by the Flash Card. For each command, the Command Block register contents for the command invoked by the Host, and the Command Block registers updated by the Flash Card after command completion, are shown. Following is an example of the command description, showing the conventions used for each command description. Throughout this document, the terms 'Task File' and 'Command Block' are used interchangeably to refer to the ATA I/O registers

A detailed description of the execution of the command is provided. This is followed by two tables, the first showing the requirements of the Command Block registers at the time that the Host issues the command to the Flash card, and the second showing the contents of the Command Block after completion or termination on error of the command.

Command Block Specified by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	Command Code							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
SECTOR COUNT	The number of sectors/logical blocks to tranfer							
FEATURES	Set Features Code							

The preceding table represents the contents of the Command Block registers when the command is issued by the Host. Where applicable, the Host first writes the appropriate data into the Features, Sector Count, Sector Number, Cylinder Hi/Low, and Drive/Head registers, and lastly, writes the command code into the Command register. The act of writing to the command register causes the Flash card to execute the command based on the contents of the Command Block at that instance.

Note that bits 7 and 5 of the Drive/Head register are denoted as 'nu.' Although the Host is expected to always set these bits to 1 when the command is issued, the Flash card ignores the value of these bits.

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Command Block specified by Flash card upon completion/termination of 'Sample' command								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	na	na	D na	H[3:0] or LBA[27:24] of the last good sector transferred			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the last good sector transferred							
SECTOR COUNT	The number of sectors that were not transferred if an unrecoverable error occured							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TKONF	AMNF
	V	V	0	V	0	V	0	0

The above table represents the contents of the Command Block registers upon completion of the command by the Flash card.

At the completion of every command, specific bits in the Status register is as follows: the BuSY, DriveWriteFault, DataReQuest, and InDeX bits are always de-asserted, while the DriveReaDY, and DriveSeekComplete bits are always asserted. The CORRected ECC bit and the ERRor bit are set or cleared as appropriate.

The contents of the Error register are always set to zero when a command is received, and are only valid if the ERR bit in the Status register is set to '1' at the completion of a command. In addition, the MediaChange, MediaChangeRequest, TracK0NotFound, and AddressMarkNotFound bits are always cleared, regardless of the state of the ERR bit in the Status register.

For the Command Block tables, explanations for each possible code are shown below:

L (LBA Mode bit)	This bit is used to specify whether the requested sector is addressed in the LBA mode or in the Cylinder-Head-Sector, CHS, mode. When set, the LBA mode is specified. The LBA is comprised of the lower significant nibble in the Drive/Head register, LBA[27:24], concatenated with the contents of the Cylinder Hi/Lo, and the Sector registers, LBA[23:0], respectively. If L=0, the sector is addressed in the classic Cylinder/Head/Sector CHS mode.
D (Drive Select bit)	This bit is used to select card 0 or 1, allowing up to two cards to share a single Task File. If two PC Card ATA cards are present in the system, one of the cards may be assigned as copy 0, and the second card may be assigned as copy 1, using the Copy field of the PCMCIA Socket & Copy card configuration register. In this case, the card designated as Copy 0 is selected when D=0. Conversely, the card designated as Copy 1 is selected when D=1.
1 (Bit is Set)	When referring to the Command Block registers when the Host issues a command, this bit must be set to a 1 by the Host before command invocation. When referring to the Command Block contents read by the Host after completion of a command, this bit is set by the Flash card upon command completion.
0 (Bit is Cleared)	When referring to the Command Block registers when the Host issues a command, this bit must be cleared to 0 by the Host before command invocation. When referring to the Command Block contents read by the Host after completion of a command, this bit is cleared by the Flash card upon command completion.
nu (Not Used)	Although the Host may specify this register/bit when invoking the command, the value for this command block register or bit is ignored by the card.
V (Valid Data)	When referring to the Command Block contents read by the Host after completion of a command, the value for the applicable bit is specified by the card.
na (Not Affected)	The value for this bit, or register, is neither set nor cleared by the card; i.e., it is unchanged by the card after command completion.

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4.3 Identify Drive Definition

This command passes to the Host one sector of data describing the Flash card's parameters. See Table for a detailed description of the Identify Drive data.

Identify Drive Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	ECh							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified by Flash card upon completion/termination of Identify Drive command (50h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	0	0	V
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TKONF	AMNF
	0	0	0	0	0	0	0	0

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Identify Drive Information		
Word	Data	Description
0	848Ah	General configuration – signature for the PCMCIA Card
	044Ah	General configuration – Bit Significant with ATA-4 definitions
1	Note 1	Number of Cylinders
2	0000h	Reserved
3	Note 1	Number of Heads
4-5	0000h	Obsolete
6	Note 1	Number of sectors per track
7-8	0000h 0000h	Number of sectors per card (Word 7 = MSW, Word 8 = LSW)
9	0000h	Obsolete
10-19	XXXXh	20 ASCII char serial number. Words 10-19 are filled with 20 ASCII 'space' chars.
20	0002h	Obsolete
21	0002h	Obsolete
22	0004h	Number of ECC bytes passed on Read/Write Long Commands
23-26	xxxx	Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	[Manufacturer's info]	Model: SMART CF
47	8001h	Maximum number of sectors on Read/Write Multiple command
48	0000h	Reserved
49	0300h	Capabilities: LBA supported, DMA supported
50	0000h	Reserved
51	0200h	PIO data transfer cycle timing mode (PIO Mode 2)
52	0000h	Obsolete
53	0007h	Words 54-58 are valid, Word 88 is valid
54	Note 1	Number of Current Cylinders
55	Note 1	Number of Current Heads
56	Note 1	Number of Current Sectors Per Track
57-58	Note 1	Current Capacity in Sectors Word 57 = LSW, Word 58 = MSW
59	0101h	Current Setting for Block Count=1 for R/W Multiple Commands
60-61	Note 1	Total number of user addressable LBA's
62	0000h	Reserved
63	0007h	Multiword DMA Mode 0,1, & 2 supported
64	0003h	Multiword DMA Mode 3 & 4 supported
65	0078h	Minimum MW DMA transfer cycle time per word (120ns)
66	0078h	Recommended MW DMA transfer cycle time (120ns)
67	0078h	Minimum PIO transfer cycle time without flow control (120ns)

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Identify Drive Information (cont)		
Word	Data	Description
68	0078h	Minimum PIO transfer cycle time w/IORDY flow control (120ns)
69-81	0000h	Reserved
82	7009h	Command Set Support 0 Support S.M.A.R.T. Feature Set Support WRITE BUFFER command Support READ BUFFER command Support NOP command
83	400Ch	Command Set Support 1 Support CFA feature set Support Advanced Power Management feature set
84	4002h	Command Set Support 2 Support S.M.A.R.T. self test
85	0001h	Command Set Enable 0 S.M.A.R.T. feature set enabled
86	0000h	Command Set Enable 1
87	4002h	Command Set Enable 2 Enable S.M.A.R.T. self test
88	003Fh	Ultra DMA Mode 0 – 5 Supported
89	0000h	Time required for Security erase unit completion
90	0000h	Time required for Enhanced Security erase unit completion
91	0000h	Current Advanced power management value
92-127	0000h	Reserved
128	0000h	Security status
129-159	0000h	Vendor unique bytes
160	81F4h	Power requirement description 500mA Maximum
161	0000h	Reserved for assignment by the CFA
162	0000h	Key management schemes supported
163	0492h	CF Advanced True IDE Timing Mode Capability and Setting
164	001Bh	CF Advanced PC Card I/O and Memory Timing Mode Capability
165-175	0000h	Reserved for assignment by the CFA
176-255	0000h	Reserved

Note 1: This value is dependent upon the total capacity of the specific flash card.

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5 Card Information Structure

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
00h	01	CISTPL_DEVICE								Device Info Tuple	Tuple Code
02h	04	CISTPL_LINK								Link is 4 bytes	Link to next Tuple
04h	DF	Device Type Code Dh = I/O				W 1	Device Speed 111			I/O Device, No WP Speed=Extended	Device ID WPS, Device Speed
06h	79	X	F == 8.0				1 = 10 ns			80 nsec	Extended Speed
08h	01	00h == 1x					1 == 2k			2KB of address space	Device Size
0Ah	FF	List End Marker								End of Devices	End Marker
0Ch	1C	CISTPL_DEVICE_OC								Device other condition Tuple	Tuple Code
0Eh	05	CISTPL_LINK								Link is 5 bytes	Link to next Tuple
10h	02	Reserved 0						3 1	W 0	3.3V operation Wait not used	3.3V operation
12h	DF	Device Type Code Dh = I/O				W 1	Device Speed 111			I/O Device, No WP Speed=Extended	Device ID WPS, Device Speed
14h	79	X	F == 8.0				1 = 10 ns			80 nsec	Extended Speed
16h	01	00h == 1x					1 == 2k			2KB of address space	Device Size
18h	FF	List End Marker								End of Devices	End of Marker
1Ah	18	CISTPL_JEDEC_C								JEDEC ID Common Memory	Tuple Code
1Ch	02	CISTPL_LINK								Link is 2 bytes	Link to next Tuple
1Eh	DF	PCMCIA Manufacturer's ID									Byte 1, JEDEC ID of Device 1
20h	01	PCMCIA Code for PC card ATA no Vpp Required								Second Byte of JEDEC ID	Byte 2 JEDEC ID
22h	20	CISTPL_MANFID								Manufacturing ID	Tuple Code
24h	04	CISTPL_LINK								Link is 4 bytes	Link to next Tuple
26h	7F	Card Manufacturer's Code								Smart JEDEC Manufacturer's ID	TPLMID_MANF
28h	94										TPLMID_MANF
2Ah	07	Manufacturer's Information									TPLMID_MANF
2Ch	00										TPLMID_MANF

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Card Information Structure (cont)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
2Eh	15	CISTPL_VERS_1								Level 1 version	Tuple Code
30h	23	CISTPL_LINK								Link is 33 bytes	Link to next Tuple
32h	04	TPPLV_MAJOR								PCMCIA 2.0/ JEIDA 4.1	Major Version
34h	01	TPPLV_MINOR								PCMCIA 2.0/ JEIDA 4.1	Minor Version
36h	53	ASCII Manufacturing String								S	Info String 1
38h	4D									M	
3Ah	41									A	
3Ch	52									R	
3Eh	54									T	
40h	20										
42h	4D									M	
44h	4F									O	
46h	44									D	
48h	55									U	
4Ah	4C									L	
4Ch	41									A	
4Eh	52									R	
50h	20										
52h	54									T	
54h	45									E	
56h	43									C	
58h	48									H	
5Ah	00									.	
5Ch	53									S	
5Eh	4D									M	
60h	41									A	
62h	52									R	

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Card Information Structure (cont)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
68h	32									2	
6Ah	32									2	
6Ch	32									3	
6Eh	20										
70h	43									C	
72h	46									F	
74h	00									.	
76h	FF	List End Marker								End of Devices	End of Marker
78h	21	CISTPL_FUNCID								Control ID Tuple	Tuple Code
7Ah	02	CISTPL_LINK								Link is 2 bytes	Link to next Tuple
7Ch	04	IC Card Function Code								FIXED DISK Function	TPLFID_FUNCTION
7Eh	01	R0	R0	R0	R0	R0	R0	R0	P1	Attempt installation at Post P: Install at POST R: Reserved	
80h	22	CISTPL_FUNCE								Function Extension Tuple	Tuple Code
82h	02	CISTPL_LINK								Link is 2 bytes	Link to next Tuple
84h	01	Disk Function Extension Tuple Type								Disk Device interface	TPLFE_TYPE

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Card Information Structure (cont)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
86h	01	Interface Type Code								PC Card-ATA interface	TPLFE_DATA
88h	22	CISTPL_FUNCE								Function Extension Tuple	Tuple Code
8Ah	03	CISTPL_LINK								Link is 3 bytes	Link to next Tuple
8Ch	02	Disk Function Extension Tuple Type								PCMCIA-ATA Extension Tuple	Extension Tuple Type for Disk
8Eh	0C	R 0	R 0	R 0	R 0	U 1	S 1	V 0		Silicon Drive V:0 No Vpp required S:Silicon U:ID Drive not Mfg/SN unique R:Reserved	TPLFE_DATA
90h	0F	R 0	I 0	E 0	N 0	P3 1	P2 1	P1 1	P0 1	Sleep,Standby, Idle Mode supported P0:Sleep Mode supported P1:Standy Mode supported P2:Idle Mode supported P3:Drive Auto Power Control not supported N:Same Primary or Secondary I/O addressing exclude 3F7H E: Index bit Not Emulated I: IOIS16 is asserted on Twin configuration R:Reserved	
92h	1A	CISTPL_CONFIG								Configuration Tuple	Tuple Code
94h	05	CISTPL_LINK								Link is 5 bytes	Link to next Tuple

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Card Information Structure (cont)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
96h	01	RFSZ 00		RMSZ 0000				RASZ 01		Size of Field RFSZ:reserved Field RMSZ: Reg Mask RASZ: Base Address	TPCC_SZ
98h	03	TPCC_LAST								Entry Index 03h	Last entry of Configuration table
9Ah	00	TPCC_RADR (LSB)								Configuration Registers are located at 200h	Location of Config Registers
9Ch	02	TPCC_RADR (MSB)									
9Eh	0F	R 0	R 0	R 0	R 0	S 1	P 1	C 1	I 1	4 Configuration registers are present I: Configuration Index C: Configuration & Status P: Pin replacement S: Socket and Copy R: Reserved for future	TPCC_RMSK
A0h	1B	CISTPL_CFTABLE_ENTRY								Configuration Entry Tuple	Tuple Code
A2h	08	CISTPL_LINK								Link is 8 bytes	Link to next Tuple
A4h	C0	I 1	D 1	Configuration Index 000000						Memory Mapped I/O D: Default Configuration I: Interface Byte Follows	TPCE_INDEX
A6h	C0	W 1	R 1	P 0	B 0	Interface Type 0000				Interface: Memory only BVD & WP not used, RDY/BSY# & Wait# used for Memory Cycle B: Battery Volt detects P: Write Protect R: RDY/BSY# W: Wait used for Memory Cycle	TPCE_IF
A8h	A1	M 1	MS 01		IR 0	IO 0	T 0	P 01		VCC-Power-description structure only P: Power info type T: Timing info not present I/O: I/O port info not present IR: Interrupt info not present MS: Mem space info type M: misc. info bytes present	TPCE_FS

Card Information Structure (cont)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
AAh	01	R 0	DI 0	PI 0	AI 0	SI 0	HV 0	LV 0	NV 1	Nominal operating supply voltage. NV: Nominal Voltage	Power Parameters for Vcc
ACh	55	X 0	Ah = 5.0				5h = 1V			Vcc Nominal is 5 Volts	Vcc Nominal Value
AEh	08	Length in 256 byte pages (LSB)								Length of Mem Space is 2KB	TPCE_MS Length LSB
B0h	00	Length in 256 byte pages (MSB)								Start at 0 on card	TPCE_MS Length MSB
B2h	20	X 0	R 0	P 1	RO 0	A 0	Twin 0			Power Down T: Twin Cards Allowed A: Audio Not Supported RO: Read only Mode P: Power-Down Supported R: Reserved X: No More Misc. Features	TPCE_MI
B4h	1B	CISTPL_CFTABLE_ENTRY								Configuration Entry Tuple	Tuple Code
B6h	06	CISTPL_LINK								Link is 6 bytes	Link to next Tuple
B8h	00									Configuration Index Byte No interface configuration byte is present following this byte	TPCE_INDX
BAh	01	M 0	MS 00		IR 0	IO 0	T 0	P 01		VCC Power-description structure only P: Power info type T: Timing info IO: I/O port info IR: Interrupt info MS: No memory space M: Misc. info bytes	TPCE_FS
BCh	21	R 0	DI 0	PI 1	AI 0	SI 0	HV 0	LV 0	NV 1	Nominal operating supply voltage NV: Nominal Voltage LV: Minimum Voltage HV: Maximum Voltage SI: Static Current AI: Average Current PI: Peak Current DI: Power Down Current	Power Parameters for VCC
BEh	B5	Mantissa Exponent								Nom Voltage = 3.0V	Vcc nominal value
C0h	1E	Extension								+0.3V	Extension byte

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Card Information Structure (cont)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
C2h	4D	Mantissa Exponent								Peak I Parameter 2.5mA	Max avg current
C4h	1B	CISTPL_CFTABLE_ENTRY								Configuration Entry Tuple	Tuple Code
C6h	0A	CISTPL_LINK								Link is 10 bytes	Link to next Tuple
C8h	C1	I 1	D 1	Configuration Index 000001						I/O Mapped Contiguous D: Default Configuration I: Interface Byte follows	TPCE_INDEX
CAh	41	W 0	R 1	P 0	B 0	Interface Type 1				I/O Interface, BVD & WP not used. RDY/BSY# used WAIT# not used	TPCE_IF
CCh	99	M 1	MS 00		IR 1	IO 1	T 0	P 01		VCC power-description structure only P: Power info type T: Timing info present IO: I/O port info present IR: Interrupt info present MS: No memory space M: Misc. info bytes present	TPCE_FS
CEh	01	R 0	DI 0	PI 0	AI 0	SI 0	HV 0	LV 0	NV 1	Nominal operating supply voltage NV: Nominal Voltage LV: Minimum Voltage HV: Maximum Voltage SI: Static Current AI: Average Current PI: Peak Current DI: Power Down Current	Power Parameters for VCC
D0h	55	X 0	Ah = 5.0				5h = 1V			VCC Nominal is 5 Volts	VCC Nominal Value
D2h	64	R 0	S 1	E 1	IO Add Lines 00100					Supports both 8/16 bit I/O accesses	TPCE_IO
D4h	F0	S 1	P 1	L 1	M 1	V 0	B 0	I 0	N 0	IRQ Sharing Logic Active Pulse & Level mode Interrupts supported IREQ 0-15 S: Share Logic Active P: pulse IRQ Supported L: Level IRQ Supported M: Bit Mask of IRQ V: Vendor Specific Signal B: Bus Error signal I: I/O check signal N: Non Maskable IRQ	TPCE_IR

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Card Information Structure (cont)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
D6h	FF	7 1	6 1	5 1	4 1	3 1	2 1	1 1	0 1	IRQ Levels to be routed 0~7 recommended	TPCE_IR Mask Extension
D8h	FF	F 1	E 1	D 1	C 1	B 1	A 1	9 1	8 1	IRQ Levels to be routed 8~15 recommended	TPCE_IR Mask Extension
DAh	20	X 0	R 0	P 1	RO 0	A 0	Twin 000			Power Down Supported T: Twin Cards Allowed A: Audio Not Supported RO: Read Only Mode P: Power Down R: Reserved X: More Misc. Fields Byte	TPCE_MI
DCh	1B	CISTPL_CFTABLE_ENTRY								Configuration Entry Tuple	Tuple Code
DEh	06	CISTPL_LINK								Link is 6 bytes	Link to next Tuple
E0h	01									Configuration Index Byte No interface configuration byte is present following this byte	TPCE_INDX
E2h	01	M 0	MS 00		IR 0	IO 0	T 0	P 01		VCC Power-description structure only P: Power info type T: Timing info IO: I/O port info IR: Interrupt info MS: No memory space M: Misc info bytes	TPCE_FS
E4h	21	R 0	DI 0	PI 1	AI 0	SI 0	HV 0	LV 0	NV 1	Nominal operating supply votage NV: Nominal Voltage LV: Minimum Voltage HV: Maximum Voltage SI: Static Current AI: Average Current PI: Peak Current DI: Power Down Current	Power Parameters for VCC
E6h	B5	Mantissa Exponent								Nom Voltage =3.0V	Vcc nominal value
E8h	1E	Extension								+0.3V	Extension byte
EAh	4D	Mantissa Exponent								Peak I Parameter 2.5mA	Max avg current
ECh	1B	CISTPL_CFTABLE_ENTRY								Configuration Entry Tuple	Tuple Code
EEh	0F	CISTPL_LINK								Link is 16 bytes	Link to next tuple

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Card Information Structure (cont)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
F0h	C2	I 1	D 1	Configuration Index 000010						I/O Mapped Contiguous D: Default Configuration I: Interface Byte follows	TPCE_INDX
F2h	41	W 0	R 1	P 0	B 0	Interface Type 1				I/O Interface, BVD & WP not used. RDY/BSY# used WAIT# not used	TPCE_IF
F4h	99	M 1	MS 00		IR 1	IO 1	T 0	P 01		VCC-Power-description structure only P: Power info type T: Timing info present IO:I/O port info present IR: Interrupt info not present MS: No Mem space M: Misc. info bytes present	TPCE_FS
F6h	01	R 0	DI 0	PI 1	AI 0	SI 0	HV 1	LV 1	NV 1	Nominal operating supply voltage NV: Nominal Voltage LV: Minimum Voltage HV: Maximum Voltage SI: Static Current AI: Average Current PI: Peak Current DI: Power Down Current	Power Parameters for Vcc
F8h	55	X 0	Ah = 5.0			5h = 1V				VCC Nominal is 5 Volts	VCC Nominal Value
FAh	EA	R 1	B 11			I/O 10h				I/O Space Addresses Bus 16/8: Register accesible by 8 or 16 bits I/O: A 1 kbyte I/O address space	TPCE_IO
FCh	61	L 01		A 10		I/O 01				L: Length 1 byte long A: Address is 4 bytes long	
FEh	F0									1st I/O base address (LSB)	1st I/O range address
100h	01									1st I/O base address (MSB)	
102h	07									1st I/O length - 1	1st I/O range length
104h	F6									2nd I/O base address (LSB)	2nd I/O range length
106h	03									2nd I/O base address (MSB)	
108h	01									2nd I/O length - 1	2nd I/O range length

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Card Information Structure (cont)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
10Ah	EE	S 1	P 1	L 1	M 0	V 1	B 1	I 1	N 0	IRQ Sharing Logic Active Pulse & Level mode Interrupts supported IREQ 0-15 S: Share Logic Active P: pulse IRQ Supported L: Level IRQ Supported M: Bit Mask of IRQ V: Vendor Specific Signal B: Bus Error signal I: I/O check signal N: Non Maskable IRQ	TPCE_IR
10Ch	20	X 0	R 0	P 1	RO 0	A 0	Twin 001			Power Down Supported T: Twin Cards Allowed A: Audio Not Supported RO: Read only Mode P: Power-Down Supported R: Reserved X: No More Misc Features	TPCE_MI
10Eh	1B	CISTPL_CFTABLE_ENTRY								Configuration Entry Tuple	Tuple Code
110h	06	CISTPL_LINK								Link is 6 bytes	Link to next Tuple
112h	02									Configuration Index Byte No interface configuration byte is present following this byte	TPCE_INDX
114h	01	M 0	MS 00		IR 0	IO 0	T 0	P 01		VCC power-description structure only P: Power info type T: Timing info IO: I/O port info IR: Interrupt info MS: No memory space M: Misc. info bytes	TPCE_FS
116h	21	R 0	DI 0	PI 1	AI 0	SI 0	HV 0	LV 0	NV 1	Nominal operating supply voltage NV: Nominal Voltage LV: Minimum Voltage HV: Maximum Voltage SI: Static Current AI: Average Current PI: Peak Current DI: Power Down Current	Power Parameters for VCC
118h	B5	Mantissa Exponent								Nom Voltage = 3.0V	Vcc nominal value
11Ah	1E	Extension								+0.3V	Extension byte

Card Information Structure (cont)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
11Ch	4D	Mantissa Exponent								Peak I Parameter 2.5mA	Max avg current
11Eh	1B	CISTPL_CFTABLE_ENTRY								Configuration Entry Tuple	Tuple Code
120h	0F	CISTPL_LINK								Link is 18 bytes	Link to next tuple
122h	C3	I 1	D 1	Configuration Index 000011						I/O Mapped Contiguous D: Default Configuration I: Interface Byte follows	TPCE_INDX
124h	41	W 0	R 1	P 0	B 0	Interface Type 1				I/O Interface, BVD & WP not used. RDY/BSY# used WAIT# not used	TPCE_IF
126h	99	M 1	MS 00		IR 1	IO 1	T 0	P 01		VCC-Power-description structure only P: Power info type T: Timing info present IO:I/O port info present IR: Interrupt info not present MS: No Mem space M: Misc. info bytes present	TPCE_FS
128h	01	R 0	DI 0	PI 1	AI 0	SI 0	HV 1	LV 1	NV 1	Nominal operating supply voltage NV: Nominal Voltage LV: Minimum Voltage HV: Maximum Voltage SI: Static Current AI: Average Current PI: Peak Current DI: Power Down Current	Power Parameters for Vcc
12Ah	55	X 0	Ah = 5.0			5h = 1V				Vcc Nominal is 5 Volts	Vcc Nominal Value
12Ch	EA	R 1	B 11			I/O 10h				I/O Space Addresses Bus 16/8: Register accesible by 8 or 16 bits I/O: A 1 kbyte I/O address space	TPCE_IO
12Eh	61	L 01		A 10		I/O 01				L: Length 1 byte long A: Address is 4 bytes long	
130h	70									1st I/O base address (LSB)	1st I/O range address
132h	01									1st I/O base address (MSB)	
134h	07									1st I/O length - 1	1st I/O range length
136h	76									2nd I/O base address (LSB)	2nd I/O range length

Card Information Structure (cont)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
138h	03									2nd I/O base address (MSB)	
13Ah	01									2nd I/O length - 1	2nd I/O range length
13Ch	EE	S 1	P 1	L 1	M 0	V 1	B 1	I 1	N 0	IRQ Sharing Logic Active Pulse & Level mode Interrupts supported IREQ 0-15 S: Share Logic Active P: pulse IRQ Supported L: Level IRQ Supported M: Bit Mask of IRQ V: Vendor Specific Signal B: Bus Error signal I: I/O check signal N: Non Maskable IRQ	TPCE_IR
13Eh	20	X 0	R 0	P 1	RO 0	A 0	Twin 001			Power Down Supported T: Twin Cards Allowed A: Audio Not Supported RO: Read only Mode P: Power-Down Supported R: Reserved X: No More Misc Features	TPCE_MI
140h	1B	CISTPL_CFTABLE_ENTRY								Configuration Entry Tuple	Tuple Code
142h	06	CISTPL_LINK								Link is 6 bytes	Link to next Tuple
144h	03									Configuration Index Byte No interface configuration byte is present following this byte	TPCE_INDX
146h	01	M 0	MS 00		IR 0	IO 0	T 0	P 01		VCC power-description structure only P: Power info type T: Timing info IO: I/O port info IR: Interrupt info MS: No memory space M: Misc. info bytes	TPCE_FS
148h	21	R 0	DI 0	PI 1	AI 0	SI 0	HV 0	LV 0	NV 1	Nominal operating supply voltage NV: Nominal Voltage LV: Minimum Voltage HV: Maximum Voltage SI: Static Current AI: Average Current PI: Peak Current DI: Power Down Current	Power Parameters for VCC

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Card Information Structure (cont)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
14Ah	B5	Mantissa Exponent								Nom Voltage = 3.0V	Vcc nominal value
14Ch	1E	Extension								+0.3V	Extension byte
14Eh	4D	Mantissa Exponent								Peak I Parameter 2.5mA	Max avg current
150h	14	CISTPL_NO_LINK								No Link Tuple	Tuple Code
152h	00	No Bytes Following								Link is 0 bytes	Link to next Tuple
154h	FF	CISTPL_END								End of list Tuple	Tuple Code

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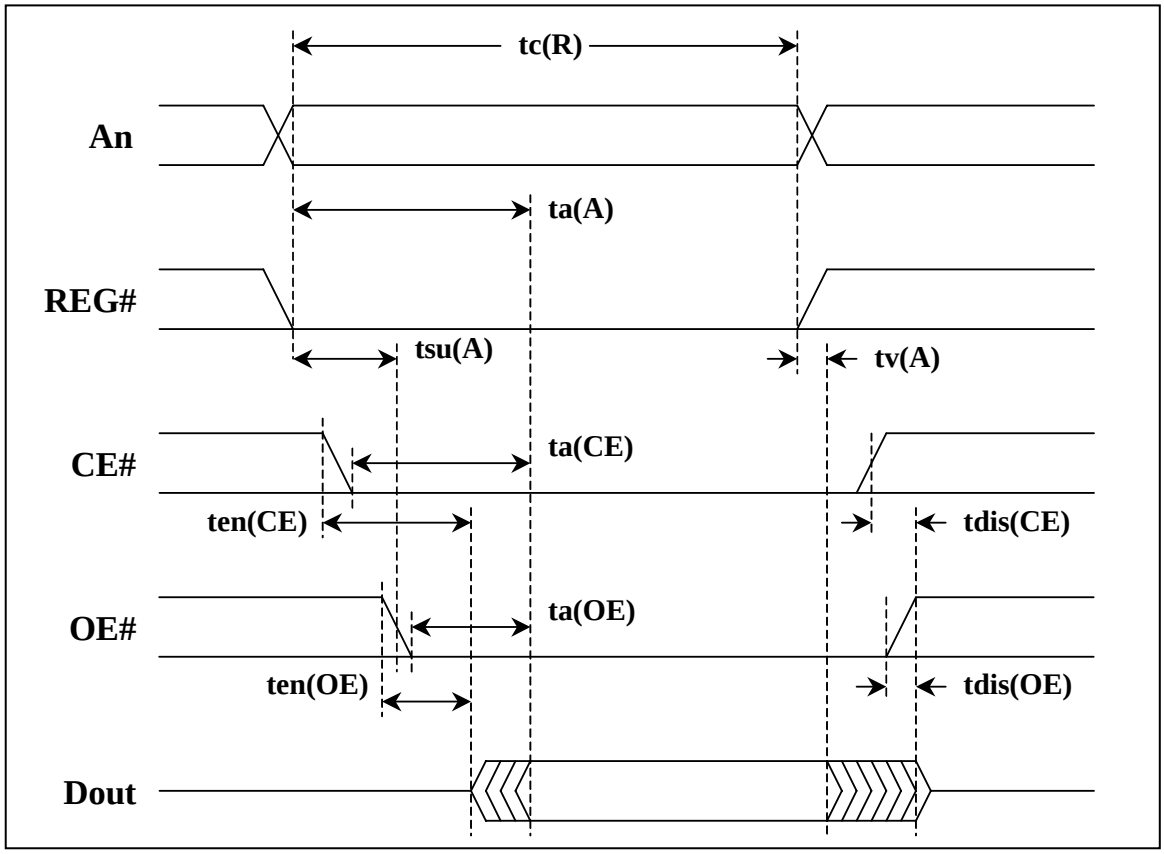
6 Timing Information

6.1.1 Attribute Memory Read Timing

Item	Symbol	IEEE Symbol	Min (ns)	Max (ns)
Read Cycle Time	tc(R)	tAVAV	300	
Address Access Time	ta(A)	tAVQV		300
Card Enable Access Time	ta(CE)	tELQV		300
Output Enable Access Time	ta(OE)	tGLQV		150
Output Disable Time from CE	tdis(CE)	tEHQZ		100
Output Disable Time from OE	tdis(OE)	tGHQZ		100
Address Setup Time	tsu(A)	tAVWL	30	
Output Enable Time from CE	ten(CE)	tELQNZ	5	
Output Enable Time from OE	ten(OE)	tGLQNZ	5	
Data Valid from Address Change	tv(A)	tAXZX	0	



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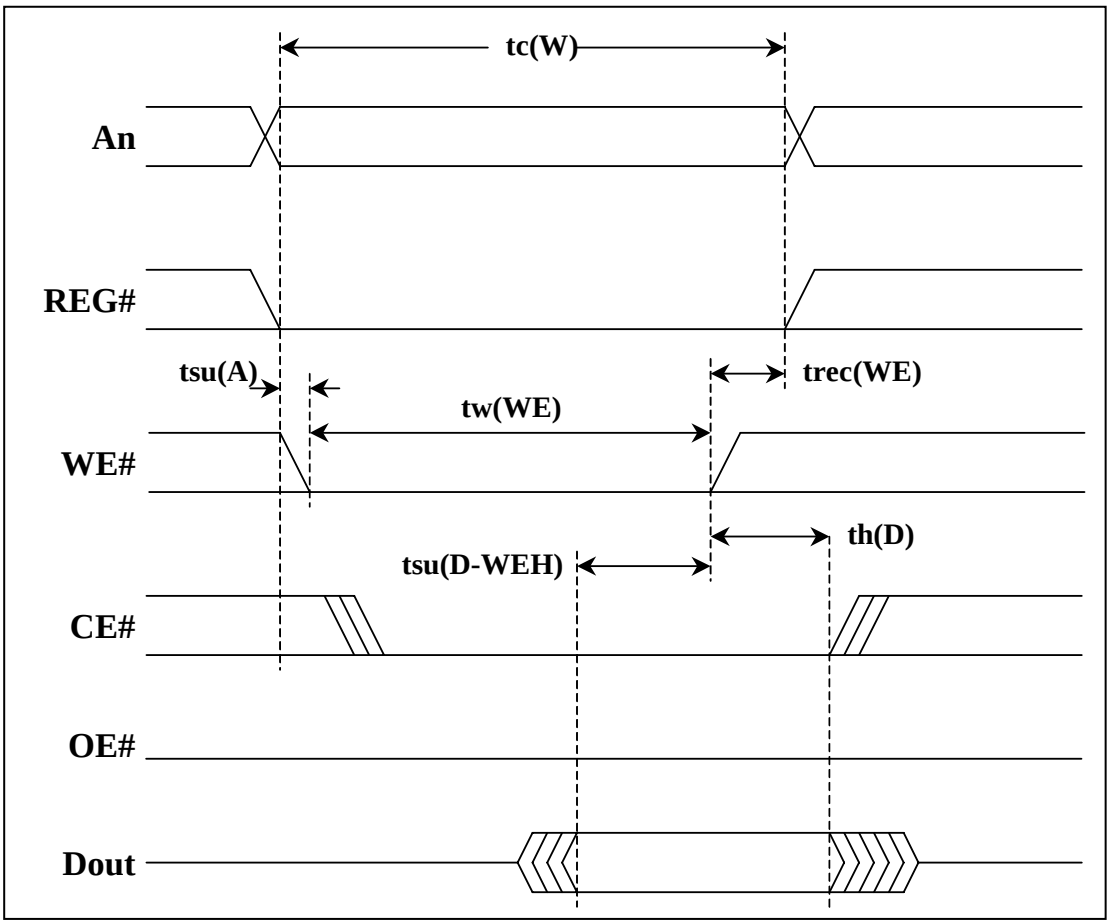
6.1.2 Attribute Memory Write Timing

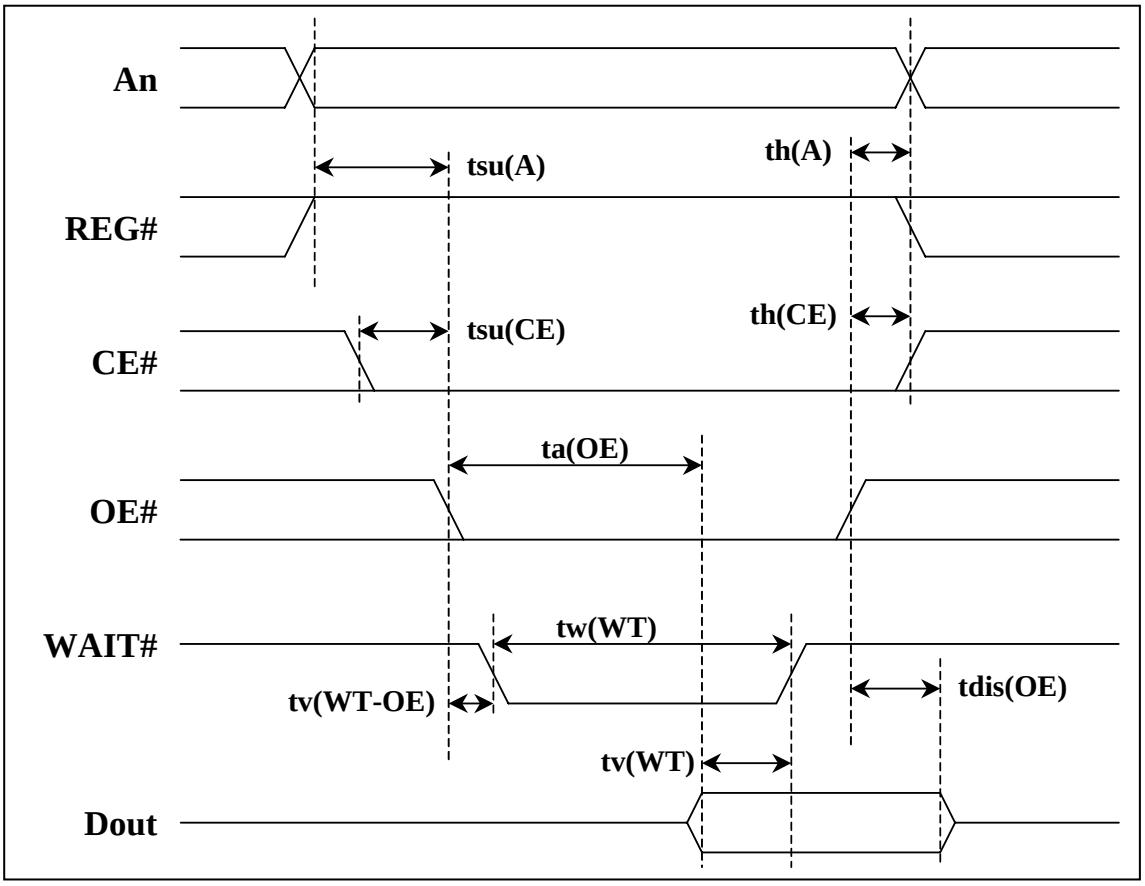
Item	Symbol	IEEE Symbol	Min (ns)	Max (ns)
Write Cycle Time	tc(W)	tAVAV	250	
Write Pulse Width	tw(WE)	tWLWH	150	
Address Setup Time	tsu(A)	tAVWL	30	
Write Recovery Time	trec(WE)	tWMAX	30	
Data Setup Time for WE	tsu(D-WEH)	tDVWH	80	
Data Hold Time	th(D)	tWMDX	30	



6.1.3 Common Memory Read Timing

Cycle Time Mode:		250 ns		120 ns		100 ns		80 ns	
Item	**Symbol**	**Min (ns)**	**Max (ns)**	**Min (ns)**	**Max (ns)**	**Min (ns)**	**Max (ns)**	**Min (ns)**	**Max (ns)**
Output Enable Access Time	ta(OE)		125		60		50		45
Output Disable Time from OE	tdis(OE)		100		60		50		45
Address SetupTime	tsu(A)	30		15		10		10	
Address Hold Time	th(A)	20		15		15		10	
CE Setup before OE	tsu(CE)	0		0		0		0	
CE Hold following OE	th(CE)	20		15		15		10	
Wait Delay Falling from OE	tv(WT-OE)		35		35		35		na[1]
Data Setup for Wait Release	tv(WT)		0		0		0		na[1]
Wait Width Time[2]	tw(WT)		350		350		350		na[1]

Notes: 1. WAIT# is not supported in this mode
2. The WAIT# signal may be ignored if the OE# cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the CIS. The Wait Width time meets PCMCIA specification of 12µs but is intentionally less in this specification.

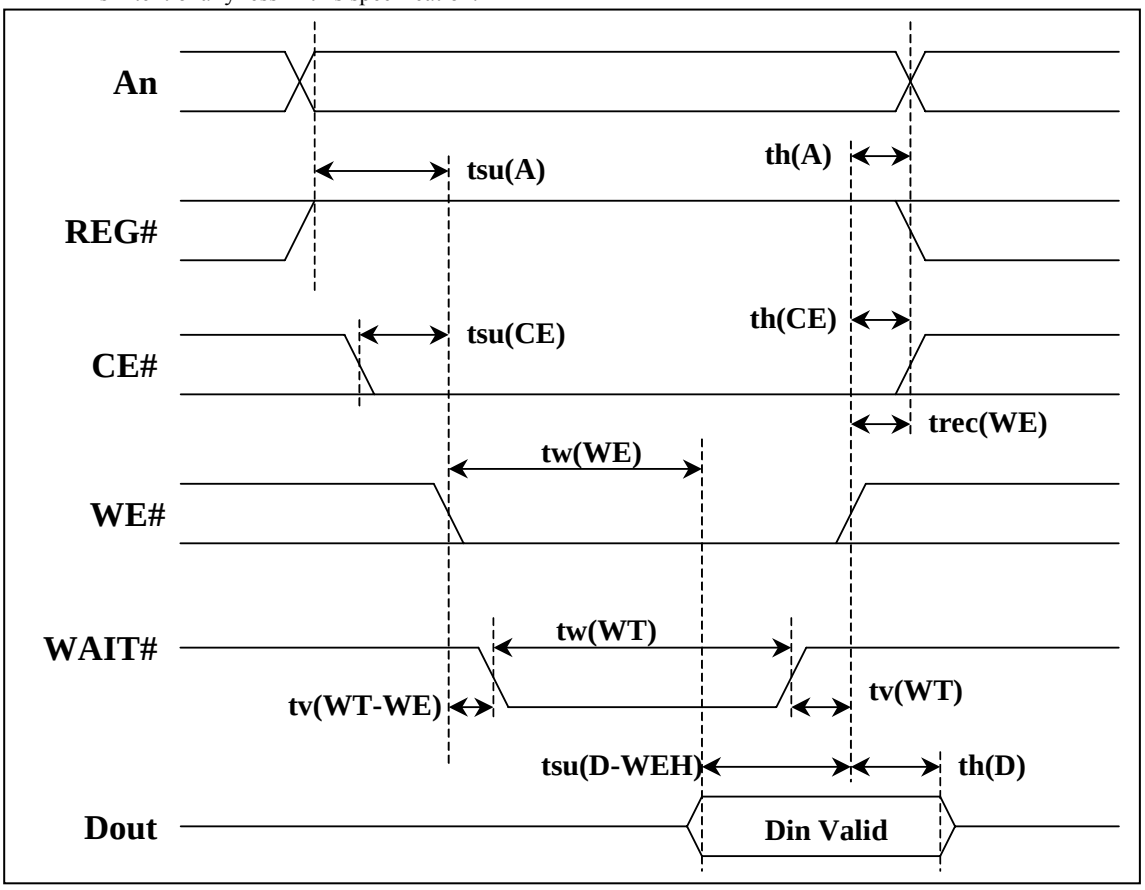


6.1.4 Common Memory Write Timing

Cycle Time Mode:		250 ns		120 ns		100 ns		80 ns	
Item	Symbol	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Data Setup before WE	tsu(D-WEH)	80		50		40		30	
Data Hold following WE	th(D)	30		15		10		10	
WE Pulse Width	tw(WE)	150		70		60		55	
Address Setup Time	tsu(A)	30		15		10		10	
CE Setup before WE	tsu(CE)	0		0		0		0	
Write Recovery Time	trec(WE)	30		15		15		15	
Address Hold Time	th(A)	20		15		15		15	
CE Hold Following WE	th(CE)	20		15		15		10	
Wait Delay Falling from WE	tv(WT-WE)		35		35		35		na[1]
WE High from Wait Release	tv(WT)	0		0		0		na[1]	
Wait Width Time	tw(WT)		350		350		350		na[1]

Notes: 1. WAIT# is not supported in this mode

2. The WAIT# signal may be ignored if the OE# cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the CIS. The Wait Width time meets PCMCIA specification of 12µs but is intentionally less in this specification.

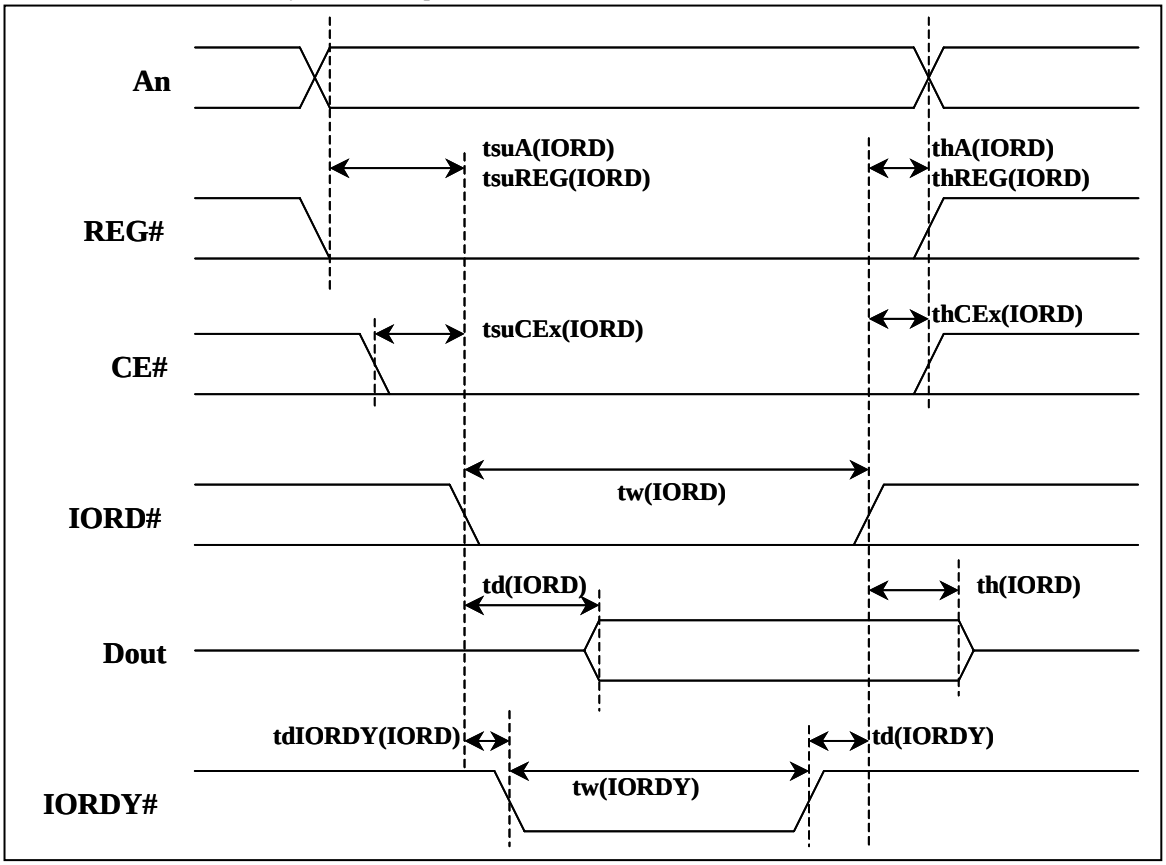


6.1.5 I/O Memory Read Timing

	Cycle Time Mode:	250 ns		120 ns		100 ns		80 ns	
Item	Symbol	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Data Delay after IORD	td(IORD)		100		50		50		45
Data Hold following IORD	th(IORD)	0		5		5		5	
IORD Width Time	tw(IORD)	165		70		65		55	
Address Setup before IORD	tsuA(IORD)	70		25		25		15	
Address Hold following IORD	thA(IORD)	20		10		10		10	
CE Setup before IORD	tsuCE(IORD)	5		5		5		5	
CE Hold following IORD	thCE(IORD)	20		10		10		10	
REG Setup before IORD	tsuREG(IORD)	5		5		5		5	
REG Hold following IORD	thREG(IORD)	0		0		0		0	
Wait Delay Falling from IORD[2]	tdIORDY(IORD)		35		35		35		na[1]
Data Delay from Wait Rising[2]	td(IORDY)		0		0		0		na[1]
Wait Width Time[2]	tw(IORDY)		350		350		350		na[1]

Notes: 1. IORDY is not supported in this mode

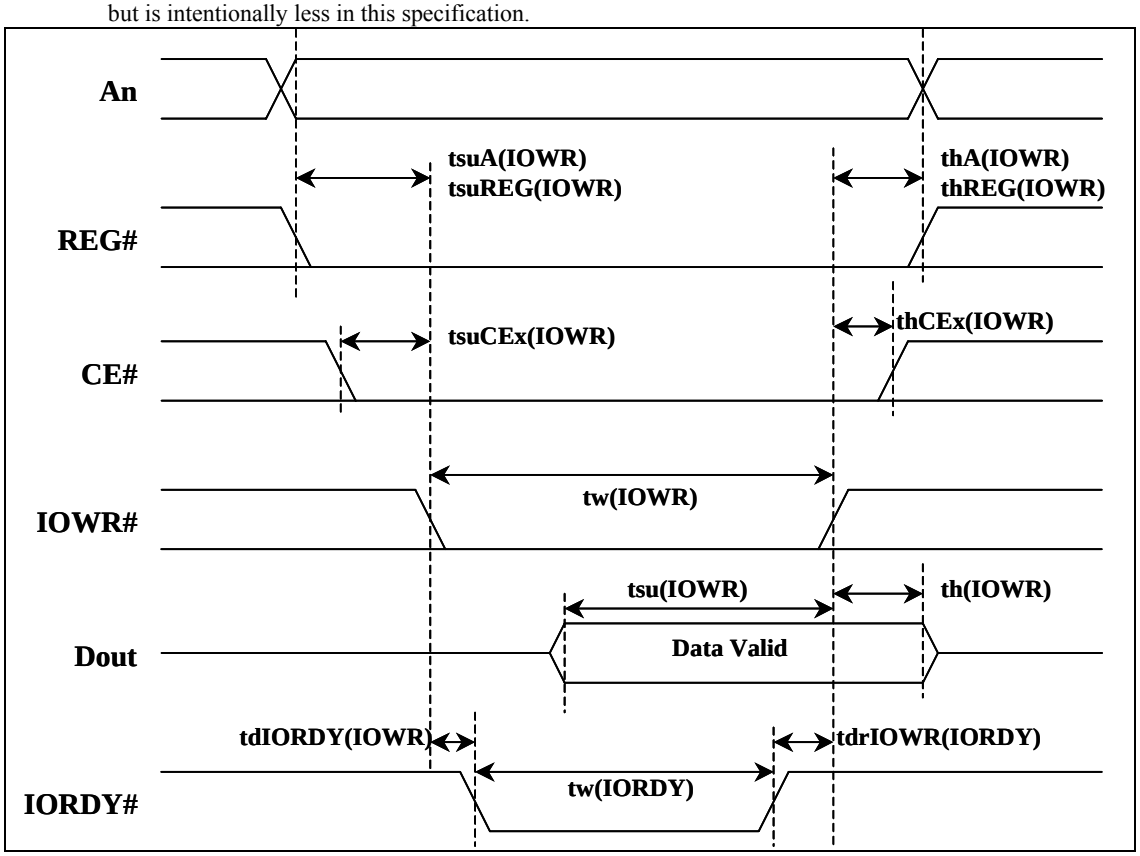
2. Minimum time from IORDY high to IORD high is 0msec, but minimum IORD width shall still be met. HD signifies data provided by the ATA Card to the system. The Wait Width time meets PCMCIA specification of 12µs but is intentionally less in this specification.



6.1.6 I/O Memory Write Timing

	Cycle Time Mode:	255 ns		120 ns		100 ns		80 ns	
Item	Symbol	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Data Setup before IOWR	tsu(IOWR)	60		20		20		15	
Data Hold following IOWR	th(IOWR)	30		10		5		5	
IOWR Width Time	tw(IOWR)	165		70		65		55	
Address Setup before IOWR	tsuHA(IOWR)	70		25		25		15	
Address Hold following IOWR	thHA(IOWR)	20		20		10		10	
CEx Setup before IOWR	tsuCEx(IOWR)	5		5		5		5	
CEx Hold following IOWR	thCEx(IOWR)	20		20		10		10	
REG# Setup before IOWR	tsuREG(IOWR)	5		5		5		5	
REG# Hold before IOWR	thREG(IOWR)	0		0		0		0	
Wait Delay Falling from IOWR[2]	tdIORDY(IOWR)		35		35		35		na[1]
IOWR high from Wait high[2]	tdrIOWR(IORDY)	0		0		0		na[1]	
Wait Width Time[2]	Tw(IORDY)		350		350		350		na[1]

Notes: 1. IORDY is not supported in this mode
2. Minimum time from IORDY high to IORD high is 0msec, but minimum IORD width shall still be met. HD signifies data provided by the ATA Card to the system. The Wait Width time meets PCMCIA specification of 12µs but is intentionally less in this specification.



6.1.7 True IDE Mode Read/Write Timing

	Item	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
t0	Cycle Time (min)	600	383	240	180	120	100	80
t1	Address Valid to HIOE/HIOW setup (min)	70	50	30	30	25	15	10
t2	IORD#/IOWR# (min)	165	125	100	80	70	65	55
t2	IORD#/IOWR# (min) Register (8 bit)	290	290	290	80	70	65	55
t2i	IORD#/IOWR#recovery time (min)	-	-	-	70	25	25	20
t3	IOWR# data setup (min)	60	45	30	30	20	20	15
t4	IOWR# data hold (min)	30	20	15	10	10	5	5
t5	IORD# data setup (min)	50	35	20	20	20	15	10
t6	IORD# data hold (min)	5	5	5	5	5	5	5
t6Z	IORD# data tristate (max)	30	30	30	30	30	20	20
t7	Address valid to IOCS16 assertion (max)	90	50	40	n/a	n/a	n/a	n/a
t8	Address valid to IOCS16 released (max)	60	45	30	n/a	n/a	n/a	n/a
t9	IORD#/IOWR#to address valid hold	20	15	10	10	10	10	10
tRD	Read Data Valid to IORDY active (min) If IORDY initially low after tA	0	0	0	0	0	0	0
tA	IORDY Setup Time	35	35	35	35	35	na	na
tB	IORDY Pulse Width (max)	1250	1250	1250	1250	1250	na	na
tC	IORDY assertion to release (max)	5	5	5	5	5	na	na

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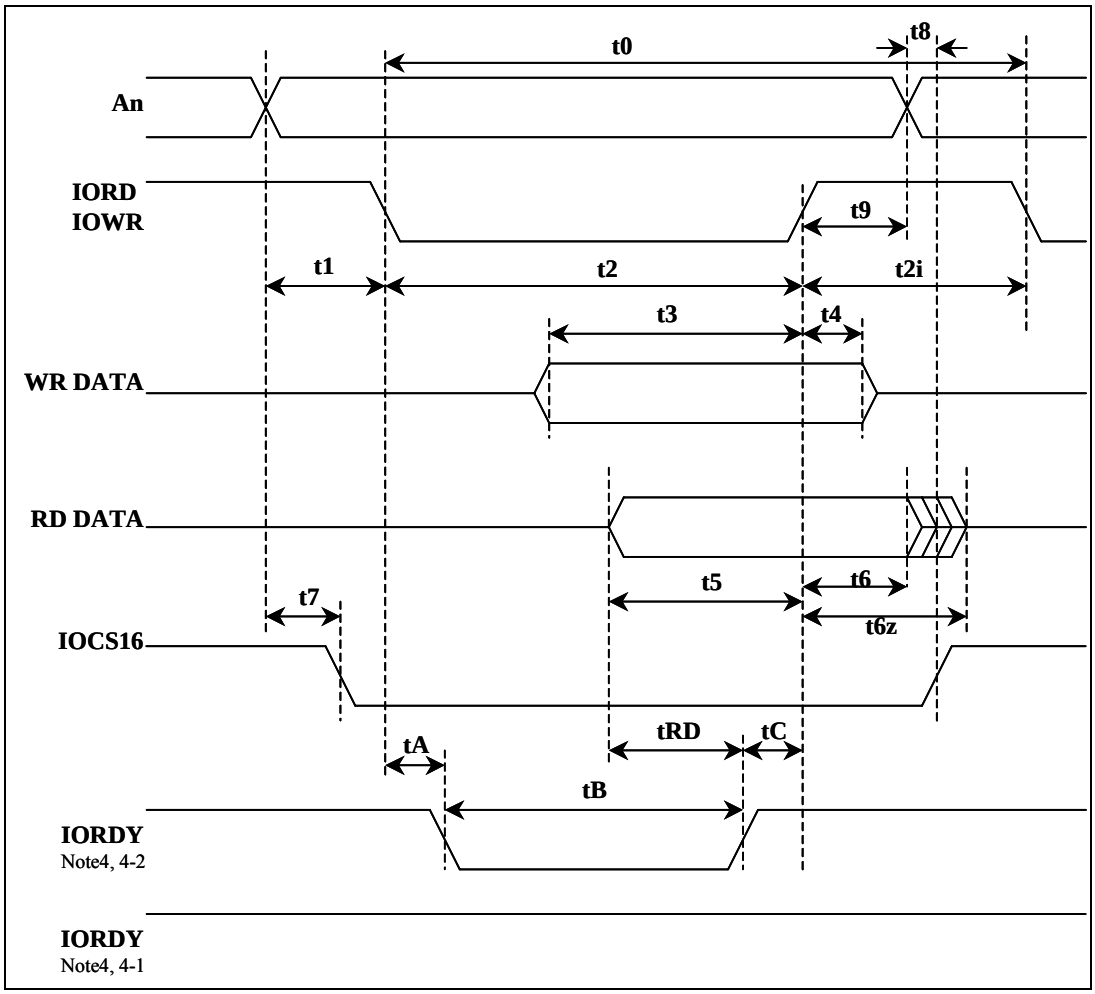
True IDE Mode Read/Write timing (cont)



True IDE Mode Read/Write Timing Diagram

Notes:
1. Device address consists of CE0, CE1, and A[2:0]
2. Data consists of D[15:0] (16-bit) or D[7:0] (8-bit)
3. IOCS16 is shown for PIO modes 0, 1, and 2. For other modes, this signal is ignored.
4. The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after tA from the assertion of IORD or IOWR. The assertion and negation of IORDY is described in the following three cases.

4-1. Device never negates IORDY: No wait is generated

4-2. Device drives IORDY low before tA: wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and IORD is asserted, the device shall place read data on D15:0 for tRD before causing IORDY to be asserted.

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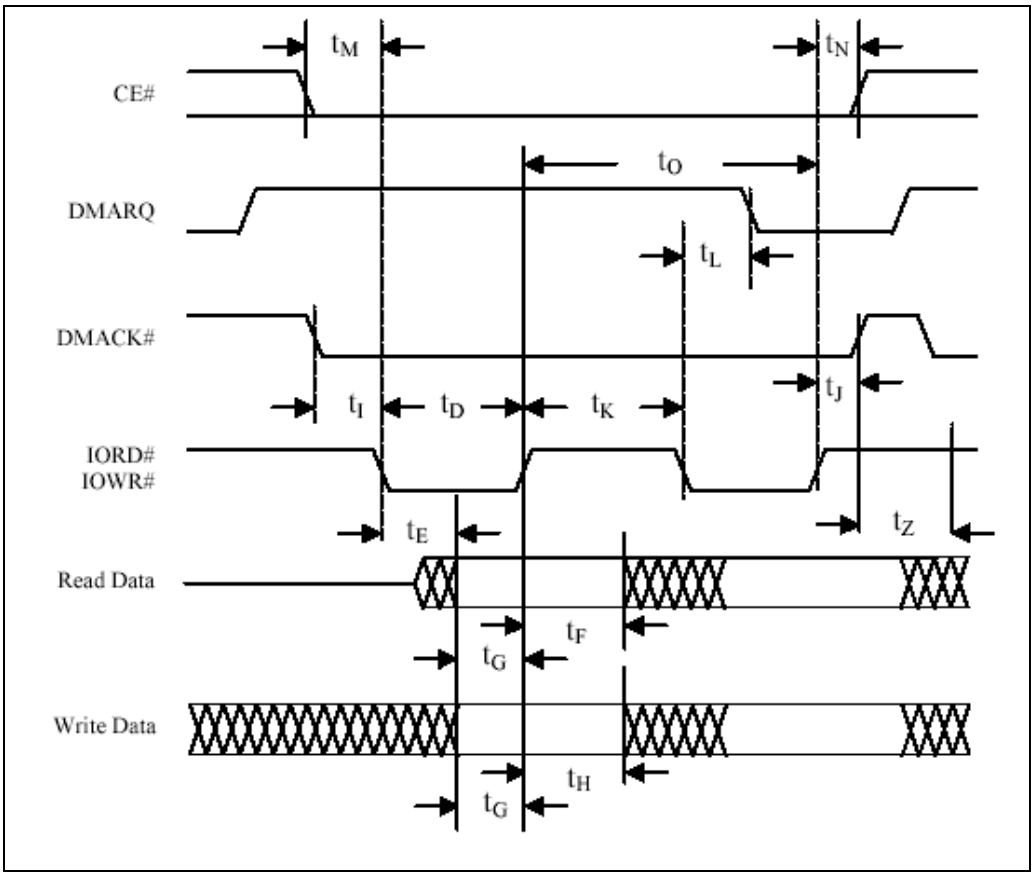
6.1.8 True IDE Multiword DMA Mode Read/Write Timing

	Item	Mode 0 (ns)	Mode 1 (ns)	Mode 2 (ns)	Mode 3 (ns)	Mode 4 (ns)
t_O	Cycle time (min)[1]	480	150	120	100	80
t_D	IORD# / IOWR# asserted width (min)[1]	215	80	70	65	55
t_E	IORD# data access (max)	150	60	50	50	45
t_F	IORD# data hold (min)	5	5	5	5	5
t_G	IORD# / IOWR# data setup (min)	100	30	20	15	10
t_H	IOWR# data hold (min)	20	15	10	5	5
t_I	DMACK# to IORD# / IOWR# setup	0	0	0	0	0
t_J	IORD# / IOWR# to –DMACK hold (min)[1]	20	5	5	5	5
t_{KR}	IORD# negated width (min)[1]	50	50	25	25	20
t_{KW}	IOWR# negated width (min)	215	50	25	25	20
t_{LR}	IORD# to DMARQ delay (max)	120	40	35	35	35
t_{LW}	IOWR# to DMARQ delay (Max)	40	40	35	35	35
t_M	CEx valid to IORD# / IOWR#	50	30	25	10	5
t_N	CEx hold	15	10	10	10	10
t_Z	DMACK#	20	25	25	25	25

Notes:
1) t_O is the minimum total cycle time and t_D is the minimum command active time, while t_{KR} and t_{KW} are the minimum command recovery time or command inactive time for input and output cycles respectively. The actual cycle time equals the sum of the actual command inactive time. The three timing requirements t_O, t_D, t_{KR}, and t_{KW} shall be met. The minimum total cycle time requirement is greater than the sum of t_D and t_{KR} or t_{KW} for input and output cycles respectively. This means a host implementation can lengthen either or both of t_D and either of t_{KR}, and t_{KW} as needed to ensure that t_O is equal to or greater than the value reported in the device's identify device data. An ATA Flash Card implementation shall support any legal host implementation.

True IDE Mode Multiword DMA Read/Write timing (cont)



Notes:

1) If the Card cannot sustain continuous, minimum cycle time DMA transfers, it may negate DMARQ within the time specified from the start of the DMA transfers in progress and reassert the signal at a later time to continue the DMA operation.
2) DMACK# may be negated by the host to suspend the DMA transfer in progress.

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6.2 Ultra DMA Mode Read/Write Timing Specification

6.3 Ultra DMA Overview

Ultra DMA is an optional data transfer protocol used with the READ DMA, and WRITE DMA, commands. When this protocol is enabled, the Ultra DMA protocol shall be used instead of the Multiword DMA protocol when these commands are issued by the host. This protocol applies to the Ultra DMA data burst only. When this protocol is used there are no changes to other elements of the ATA protocol (e.g., Command Block Register access).

Ultra DMA operations can take place in any of the three basic interface modes: PC Card Memory mode, PC Card I/O mode, and True IDE (the original mode to support UDMA). The usage of signals in each of the modes is shown in Table 22: Ultra DMA Signal Usage In Each Interface Mode.

UDMA Signal	Type	Pin# (Non UDMA MEM Mode)	PC CARD MEM MODE UDMA	PC CARD IO MODE UDMA	TRUE IDE MODE UDMA
DMARQ	Output	43 (-INPACK)	-DMARQ	-DMARQ	DMARQ
DMACK	Input	44 (-REG)	-DMACK	DMACK	-DMACK
STOP	Input	35 (-IOWR)	STOP (Note 1)	STOP (Note 1)	STOP (Note 1)
HDMARDY(R) HSTROBE(W)	Input	34 (-IORD)	-HDMARDY(R) (Note 1,2) HSTROBE(W) (Note 1, 3, 4)	-HDMARDY(R) (Note 1,2) HSTROBE(W) (Note 1, 3, 4)	-HDMARDY(R) (Note 1,2) HSTROBE(W) (Note 1, 3, 4)
DDMARDY(w) DSTROBE(R)	Output	42 (-WAIT)	-DDMARDY(w) (Note 1,3) DSTROBE(R) (Note 1,2,4)	-DDMARDY(w) (Note 1,3) DSTROBE(R) (Note 1,2,4)	-DDMARDY(w) (Note 1,3) DSTROBE(R) (Note 1,2,4)
DATA	Bidir	…(D[15:00])	D[15:00]	D[15:00]	D[15:00]
ADDRESS	Input	…(A[10:00])	A[10:00]	A[10:00]	A[02:00] (Note 5)
CSEL	Input	39 (-CSEL)	-CSEL	-CSEL	-CSEL
INTRQ	Output	37 (READY)	READY	READY	READY
Card Select	Input	7 (-CE1) 31 (-CE2)	-CE1 -CE2	-CE1 -CE2	-CS0 -CS1

Table 22: Ultra DMA Signal In Each Interface Mode

Notes:
1) The UDMA interpretation of this signal is valid only during an Ultra DMA burst.
2) The UDMA interpretation of this signal is valid only during and Ultra DMA burst during a DMA Read command.
3) The UDMA interpretation of this signal is valid only during an Ultra DMA burst during a DMA Write command.
4) The HSTROBE and DSTROBE signals are active on both the rising and the falling edge.
5) Address lines 03 through 10 are not used in True IDE mode.

Several signal lines are redefined to provide different functions during an Ultra DMA burst. These lines assume their UDMA definitions when:
1. an Ultra DMA mode is selected, and

2. a host issues a READ DMA, or a WRITE DMA command requiring data transfer, and

3. the device asserts (-)DMARQ, and

4. the host asserts (-)DMACK.

These signal lines revert back to the definitions used for non-Ultra DMA transfers upon the negation of -DMACK by the host at the termination of an Ultra DMA burst.

With the Ultra DMA protocol, the STROBE signal that latches data from D [15:00] is generated by the same agent (either host or device) that drives the data onto the bus. Ownership of D[15:00] and this data strobe signal are given either to the device during an Ultra DMA data-in burst or to the host for an Ultra DMA data-out burst.
During an Ultra DMA burst a sender shall always drive data onto the bus, and, after a sufficient time to allow for propagation delay, cable settling, and setup time, the sender shall generate a STROBE edge to latch the data. Both edges of STROBE are used for data transfers so that the frequency of STROBE is limited to the same frequency as the data.

Words in the IDENTIFY DEVICE data indicate support of the Ultra DMA feature and the Ultra DMA modes the device is capable of supporting. The Set transfer mode subcommand in the SET FEATURES command shall be used by a host to select the Ultra DMA mode at which the system operates. The Ultra DMA mode selected by a host shall be less than or equal to the fastest mode of which the device is capable. Only one Ultra DMA mode shall be selected at any given time. All timing requirements for a selected Ultra DMA mode shall be satisfied. Devices supporting any Ultra DMA mode shall also support all slower Ultra DMA modes.

An Ultra DMA capable device shall retain the previously selected Ultra DMA mode after executing a software reset sequence or the sequence caused by receipt of a DEVICE RESET command if a SET FEATURES disable reverting to defaults command has been issued. The device may revert to a Multiword DMA mode if a SET FEATURES enable reverting to default has been issued. An Ultra DMA capable device shall clear any previously selected Ultra DMA mode and revert to the default non-Ultra DMA modes after executing a power-on or hardware reset.

Both the host and device perform a CRC function during an Ultra DMA burst. At the end of an Ultra DMA burst the host sends its CRC data to the device. The device compares its CRC data to the data sent from the host. If the two values do not match, the device reports an error in the error register. If an error occurs during one or more Ultra DMA bursts for any one command, the device shall report the first error that occurred. If the device detects that a CRC error has occurred before data transfer for the command is complete, the device may complete the transfer and report the error or abort the command and report the error.

NOTE If a data transfer is terminated before completion, the assertion of INTRQ should be passed through to the host software driver regardless of whether all data requested by the command has been transferred.

6.4 Restrictions and Considerations During Ultra DMA Commands

There are number of important restrictions and considerations for the implementation and use of Ultra DMA commands in PCMCIA devices. These are highlighted in the subsections below. Additional restrictions on specific modes of operation are given in sections 4.3.7: Additional Requirements for CF Advanced Timing Modes and 4.3.18.3: Specific rules for PC Card Memory Mode Ultra DMA.

6.5 System Restrictions for Ultra DMA modes 3 and above

Ultra DMA modes 3 and above are valid only for systems that meet the requirements of section 4.3.7 Additional Requirements for CF Advanced Timing Modes

6.6 UDMA Address and Card Enable Signals

The Card Enable signals (–CE1 / –CS0 and –CE2 / –CS1) shall remain negated during Ultra DMA bursts.

The Address bus (A[10:00]) shall not transition unnecessarily during the UDMA command and shall remain fixed during an Ultra DMA burst. In True IDE mode, the address lines (A[02:00]) shall be held to all zeros. This will reduce unnecessary noise during the UDMA command.

6.7 Task File registers shall not be written during an Ultra DMA command

The task file registers shall not be written after an Ultra DMA command is issued by the host and before the command completes. Writing to the device control register is permitted between bursts, but is expected to occur only to reset the card after an unrecoverable protocol error.

6.8 Ultra DMA transfers shall be 16 bits wide

All transfers during an Ultra DMA burst are 16 bit wide transfers. The Set Features command that controls the bus width for PIO transfers does not affect the width of Ultra DMA transfers.

6.9 No Access to Memory or I/O Space during an Ultra DMA Burst

No access to common or attribute memory or to I/O space on the device is permitted during an Ultra DMA burst.

6.10 Specific rules for PC Card Memory Mode Ultra DMA

In addition to the general restrictions for all Ultra DMA operations, these additional considerations exist for PC Card Memory Mode Ultra DMA operations.

6.11 No Access to Attribute Memory during PC Card Memory Mode DMA Commands

The host shall not attempt to access Attribute Memory space during a PC Card Memory Mode DMA command either before, between or within Ultra DMA bursts.

6.12 READY signal handling during DMA commands in PC Card Memory Mode

In PC Card Memory Mode, the READY signal shall be negated (made BUSY) by the device upon receipt of a DMA command and shall remain negated until the command has completed at which time it shall be re-asserted.

This treatment allows the host to receive a single interrupt at the end of the command and avoids the extra overhead that would be associated with processing busy to ready transitions for each sector transferred as is the case when the READY toggles at the end of every sector of PIO Memory Mode transfers.

The BSY bit in the status register is permitted to be negated in the status register at any time that the DRQ bit in the status register is asserted. The only restriction is that either DRQ or BSY or both must remain asserted while the command is in progress.

6.13 Ultra DMA Phases of Operation

An Ultra DMA data transfer is accomplished through a series of Ultra DMA data-in or data-out bursts. Each Ultra DMA burst has three mandatory phases of operation: the initiation phase, the data transfer phase, and the Ultra DMA burst termination phase. In addition, an Ultra DMA burst may be paused during the data transfer phase (see: 14.3.18.5 Ultra DMA Data Transfer, for the detailed protocol descriptions for each of these phases. Table 23: Ultra DMA Data Burst Timing Requirements and Table 24: Ultra DMA Data Burst Timing Descriptions define the specific timing requirements). In the following rules -DMARDY is used in cases that could apply to either -DDMARDY or -HDMARDY, and STROBE is used in cases that could apply to either DSTROBE or HSTROBE. The following are general Ultra DMA rules.

1. An Ultra DMA burst is defined as the period from an assertion of (-)DMACK by the host during the assertion of (-)DMARQ by the device to the subsequent negation of (-)DMACK.

2. When operating in Ultra DMA modes 2, 1, or 0 a recipient shall be prepared to receive up to two data words whenever an Ultra DMA burst is paused. When operating in Ultra DMA modes 6, 5, 4, or 3 a recipient shall be prepared to receive up to three data words whenever an Ultra DMA burst is paused.

6.14 Ultra DMA Burst Initiation Phase Rules

1. An Ultra DMA burst initiation phase begins with the assertion of DMARQ by a device and ends when the sender generates a STROBE edge to transfer the first data word.

2. An Ultra DMA burst shall always be requested by a device asserting DMARQ.

3. When ready to initiate the requested Ultra DMA burst, the host shall respond by asserting-DMACK.

4. A host shall never assert -DMACK without first detecting that DMARQ is asserted.

5. For Ultra DMA data-in bursts: a device may begin driving D[15:00] after detecting that -DMACK is asserted, STOP negated, and -HDMARDY is asserted.

6. After asserting DMARQ or asserting -DDMARDY for an Ultra DMA data-out burst, a device shall not negate either signal until the first STROBE edge is generated.

7. After negating STOP or asserting -HDMARDY for an Ultra DMA data-in burst, a host shall not change the state of either signal until the first STROBE edge is generated.

6.15 Ultra DMA Data transfer phase rules

1. The data transfer phase is in effect from after Ultra DMA burst initiation until Ultra DMA burst termination.

2. A recipient pauses an Ultra DMA burst by negating -DMARDY and resumes an Ultra DMA burst by reasserting -DMARDY.

3. A sender pauses an Ultra DMA burst by not generating STROBE edges and resumes by generating STROBE edges.

4. A recipient shall not signal a termination request immediately when the sender stops generating STROBE edges. In the absence of a termination from the sender the recipient shall always negate -DMARDY and wait the required period before signaling a termination request.

5. A sender may generate STROBE edges at greater than the minimum period specified by the enabled Ultra DMA mode. The sender shall not generate STROBE edges at less than the minimum period specified by the enabled Ultra DMA mode. A recipient shall be able to receive data at the minimum period specified by the enabled Ultra DMA mode.

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6.16 Ultra DMA Burst Termination Phase Rules

1. Either a sender or a recipient may terminate an Ultra DMA burst.

2. Ultra DMA burst termination is not the same as command completion. If an Ultra DMA burst termination occurs before command completion, the command shall be completed by initiation of a new Ultra DMA burst at some later time or aborted by the host issuing a hardware or software reset or DEVICE RESET command if implemented by the device.

3. An Ultra DMA burst shall be paused before a recipient requests a termination.

4. A host requests a termination by asserting STOP. A device acknowledges a termination request by negating DMARQ.

5. A device requests a termination by negating DMARQ. A host acknowledges a termination request by asserting STOP.

6. Once a sender requests a termination, the sender shall not change the state of STROBE until the recipient acknowledges the request. Then, if STROBE is not in the asserted state, the sender shall return STROBE to the asserted state. No data shall be transferred on this transition of STROBE.

7. A sender shall return STROBE to the asserted state whenever the sender detects a termination request from the recipient. No data shall be transferred nor CRC calculated on this edge of DSTROBE.

8. Once a recipient requests a termination, the responder shall not change DMARDY from the negated state for the remainder of an Ultra DMA burst.

9. A recipient shall ignore a STROBE edge when DMARQ is negated or STOP is asserted.

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6.17 Ultra DMA Data Transfers Timing

Table 23 and Table 24 define the timings associated with all phases of Ultra DMA bursts.

Table 23: Ultra DMA Data Burst Timing Requirements

Name	UDMA Mode 0 (in ns)		UDMA Mode 1 (in ns)		UDMA Mode 2 (in ns)		UDMA Mode 3 (in ns)		UDMA Mode 4 (in ns)		UDMA Mode 5 (in ns)		UDMA Mode 6 (in ns)		Measure location (See
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Note 2)
$t_{2CYCTYP}$	240		160		120		90		60		40		30		Sender
t_{CYC}	112		73		54		39		25		16.8		13.0		Note 3
t_{2CYC}	230		153		115		86		57		38		29		Sender
t_{DS}	15.0		10.0		7.0		7.0		5.0		4.0		2.6		Recipient
t_{DH}	5.0		5.0		5.0		5.0		5.0		4.6		3.5		Recipient
t_{DVS}	70.0		48.0		31.0		20.0		6.7		4.8		4.0		Sender
t_{DVH}	6.2		6.2		6.2		6.2		6.2		4.8		4.0		Sender
t_{CS}	15.0		10.0		7.0		7.0		5.0		5.0		5.0		Device
t_{CH}	5.0		5.0		5.0		5.0		5.0		5.0		5.0		Device
t_{CVS}	70.0		48.0		31.0		20.0		6.7		10.0		10.0		Host
t_{CVH}	6.2		6.2		6.2		6.2		6.2		10.0		10.0		Host
t_{ZFS}	0		0		0		0		0		35		25		Device
t_{DZFS}	70.0		48.0		31.0		20.0		6.7		25		17.5		Sender
t_{FS}		230		200		170		130		120		90		80	Device
t_{LI}	0	150	0	150	0	150	0	100	0	100	0	75	0	60	Note 4
t_{MLI}	20		20		20		20		20		20		20		Host
t_{UI}	0		0		0		0		0		0		0		Host
t_{AZ}		10		10		10		10		10		10		10	Note 5
t_{ZAH}	20		20		20		20		20		20		20		Host
t_{ZAD}	0		0		0		0		0		0		0		Device
t_{ENV}	20	70	20	70	20	70	20	55	20	55	20	50	20	50	Host
t_{RFS}		75		70		60		60		60		50		50	Sender
t_{RP}	160		125		100		100		100		85		85		Recipient
t_{IORDYZ}		20		20		20		20		20		20		20	Device
t_{ZIORDY}	0		0		0		0		0		0		0		Device
t_{ACK}	20		20		20		20		20		20		20		Host
t_{SS}	50		50		50		50		50		50		50		Sender

Notes:

1) All timing measurement switching points (low to high and high to low) shall be taken at 1.5 V.

2) All signal transitions for a timing parameter shall be measured at the connector specified in the measurement location column. For example, in the case of tRFS, both STROBE and -DMARDY transitions are measured at the sender connector.

3) The parameter tCYC shall be measured at the recipient's connector farthest from the sender.

4) The parameter tLI shall be measured at the connector of the sender or recipient that is responding to an incoming transition from the recipient or sender respectively. Both the incoming signal and the outgoing response shall be measured at the same connector.

5) The parameter tAZ shall be measured at the connector of the sender or recipient that is driving the bus but must release the bus to allow for a bus turnaround.

6) See the AC Timing requirements in Table 26: Ultra DMA AC Signal Requirements.

Table 24: Ultra DMA Data Burst Timing Descriptions

Name	Comment	Notes
$t_{2CYCTYP}$	Typical sustained average two cycle time	
t_{CYC}	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)	
t_{2CYC}	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)	
t_{DS}	Data setup time at recipient (from data valid until STROBE edge)	2, 5
t_{DH}	Data hold time at recipient (from STROBE edge until data may become invalid)	2, 5
t_{DVS}	Data valid setup time at sender (from data valid until STROBE edge)	3
t_{DVH}	Data valid hold time at sender (from STROBE edge until data may become invalid)	3
t_{CS}	CRC word setup time at device	2
t_{CH}	CRC word hold time device	2
t_{CVS}	CRC word valid setup time at host (from CRC valid until -DMACK negation)	3
t_{CVH}	CRC word valid hold time at sender (from -DMACK negation until CRC may become invalid)	3
t_{ZFS}	Time from STROBE output released-to-driving until the first transition of critical timing.	
t_{DZFS}	Time from data output released-to-driving until the first transition of critical timing.	
t_{FS}	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)	
t_{LI}	Limited interlock time	1
t_{MLI}	Interlock time with minimum	1
t_{UI}	Unlimited interlock time	1
t_{AZ}	Maximum time allowed for output drivers to release (from asserted or negated)	
t_{ZAH}	Minimum delay time required for output	
t_{ZAD}	drivers to assert or negate (from released)	
t_{ENV}	Envelope time (from -DMACK to STOP and -HDMARDY during data in burst initiation and from DMACK to STOP during data out burst initiation)	
t_{RFS}	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of -DMARDY)	
t_{RP}	Ready-to-pause time (that recipient shall wait to pause after negating -DMARDY)	
t_{IORDYZ}	Maximum time before releasing IORDY	
t_{ZIORDY}	Minimum time before driving IORDY	4
t_{ACK}	Setup and hold times for -DMACK (before assertion or negation)	
t_{SS}	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)	

Notes:
1) The parameters tUI, tMLI (in Figure 36: Ultra DMA Data-In Burst Device Termination Timing and Figure 37: Ultra DMA Data-In Burst Host Termination Timing), and tLI indicate sender-to-recipient or recipient-to-sender interlocks, i.e., one agent (either sender or recipient) is waiting for the other agent to respond with a signal before proceeding. tUI is an unlimited interlock that has no maximum time value. tMLI is a limited time-out that has a defined minimum. tLI is a limited time-out that has a defined maximum.

2) 80-conductor cabling (see 4.3.8.4) shall be required in order to meet setup (tDS, tCS) and hold (tDH, tCH) times in modes greater than 2.

3) Timing for tDVS, tDVH, tCVS and tCVH shall be met for lumped capacitive loads of 15 and 40 pF at the connector where the Data and STROBE signals have the same capacitive load value. Due to reflections on the cable, these timing measurements are not valid in a normally functioning system.

4) For all modes the parameter tZIORDY may be greater than tENV due to the fact that the host has a pull-up on IORDY- giving it a known state when released.

5) The parameters tDS, and tDH for mode 5 are defined for a recipient at the end of the cable only in a configuration with a single device located at the end of the cable. This could result in the minimum values for tDS and tDH for mode 5 at the middle connector being 3.0 and 3.9 ns respectively.

Table 25: Ultra DMA Sender and Recipient IC Timing Requirements

Name	UDMA Mode 0 (ns)		UDMA Mode 1 (ns)		UDMA Mode 2 (ns)		UDMA Mode 3 (ns)		UDMA Mode4 (ns)		UDMA Mode 5 (ns)		UDMA Mode6 (ns)	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
t_{DSIC}	14.7		9.7		6.8		6.8		4.8		2.3		2.3	
t_{DHIC}	4.8		4.8		4.8		4.8		4.8		2.8		2.8	
t_{DVSIC}	72.9		50.9		33.9		22.6		9.5		6.0		5.2	
t_{DVHIC}	9.0		9.0		9.0		9.0		9.0		6.0		5.2	
t_{DSIC}	Recipient IC data setup time (from data valid until STROBE edge) (see note 2)													
t_{DHIC}	Recipient IC data hold time (from STROBE edge until data may become invalid) (see note 2)													
t_{DVSIC}	Sender IC data valid setup time (from data valid until STROBE edge) (see note 3)													
t_{DVHIC}	Sender IC data valid hold time (from STROBE edge until data may become invalid) (see note 3)													

Notes:
1) All timing measurement switching points (low to high and high to low) shall be taken at 1.5 V.

2) The correct data value shall be captured by the recipient given input data with a slew rate of 0.4 V/ns rising and falling and the input STROBE with a slew rate of 0.4 V/ns rising and falling at tDSIC and tDHIC timing (as measured through 1.5 V).

3) The parameters tDVSIC and tDVHIC shall be met for lumped capacitive loads of 15 and 40 pF at the IC where all signals have the same capacitive load value. Noise that may couple onto the output signals from **external** sources has not been included in these values.

Table 26: Ultra DMA AC Signal Requirements

Name	Comment	Min [V/ns]	Max [V/ns]	Notes
S_{RISE}	Rising Edge Slew Rate for any signal		1.25	1
S_{FALL}	Falling Edge Slew Rate for any signal		1.25	1

Note:
1) The sender shall be tested while driving an 18 inch long, 80 conductor cable with PVC insulation material. The signal under test shall be cut at a test point so that it has not trace, cable or recipient loading after the test point. All other signals should remain connected through to the recipient. The test point may be located at any point between the sender's series termination resistor and one half inch or less of conductor exiting the connector. If the test point is on a cable conductor rather than the PCB, an adjacent ground conductor shall also be cut within one half inch of the connector.

The test load and test points should then be soldered directly to the exposed source side connectors. The test loads consist of a 15 pF or a 40 pF, 5%, 0.08 inch by 0.05 inch surface mount or smaller size capacitor from the test point to ground. Slew rates shall be met for both capacitor values.

Measurements shall be taken at the test point using a <1 pF, >100 Kohm, 1 Ghz or faster probe and a 500 MHz or faster oscilloscope. The average rate shall be measured from 20% to 80% of the settled VOH level with data transitions at least 120 nsec apart. The settled VOH level shall be measured as the average output high level under the defined testing conditions from 100 nsec after 80% of a rising edge until 20% of the subsequent falling edge.

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6.18 Initiating an Ultra DMA Data-In Burst

a) An Ultra DMA Data-In burst is initiated by following the steps lettered below. The timing diagram is shown in Figure 33: Ultra DMA Data-In Burst Initiation Timing. The associated timing parameters are specified in Table 23: Ultra DMA Data Burst Timing Requirements and are described in Table 24: Ultra DMA Data Burst Timing Descriptions.

b) The following steps shall occur in the order they are listed unless otherwise specifically allowed:

c) The host shall keep -DMACK in the negated state before an Ultra DMA burst is initiated.

d) The device shall assert DMARQ to initiate an Ultra DMA burst. After assertion of DMARQ the device shall not negate DMARQ until after the first negation of DSTROBE.

e) Steps (c), (d), and (e) may occur in any order or at the same time. The host shall assert STOP.

f) The host shall negate -HDMARDY.

g) The host shall negate -CS0, -CS1 and A[02:00] in True IDE mode (negate –CE2, -CE1 and hold A[10:00] fixed in PC Card modes). The host shall keep -CS0, -CS1 and A[02:00] negated in True IDE mode (–CE2 and -CE1 negated and A[10:00] fixed in PC Card modes) until after negating -DMACK at the end of the burst.

h) Steps (c), (d), and (e) shall have occurred at least tACK before the host asserts -DMACK. The host shall keep -DMACK asserted until the end of an Ultra DMA burst.

i) The host shall release D[15:00] within tAZ after asserting -DMACK.

j) The device may assert DSTROBE tZIORDY after the host has asserted -DMACK. Once the device has driven DSTROBE the device shall not release DSTROBE until after the host has negated -DMACK at the end of an Ultra DMA burst.

k) The host shall negate STOP and assert -HDMARDY within tENV after asserting -DMACK. After negating STOP and asserting -HDMARDY, the host shall not change the state of either signal until after receiving the first transition of DSTROBE from the device (i.e., after the first data word has been received).

l) The device shall drive D[15:00] no sooner than tZAD after the host has asserted -DMACK, negated STOP, and asserted -HDMARDY.

m) The device shall drive the first word of the data transfer onto D[15:00]. This step may occur when the device first drives D[15:00] in step (j).

n) To transfer the first word of data the device shall negate DSTROBE within tFS after the host has negated STOP and asserted -HDMARDY. The device shall negate DSTROBE no sooner than tDVS after driving the first word of data onto D[15:00].

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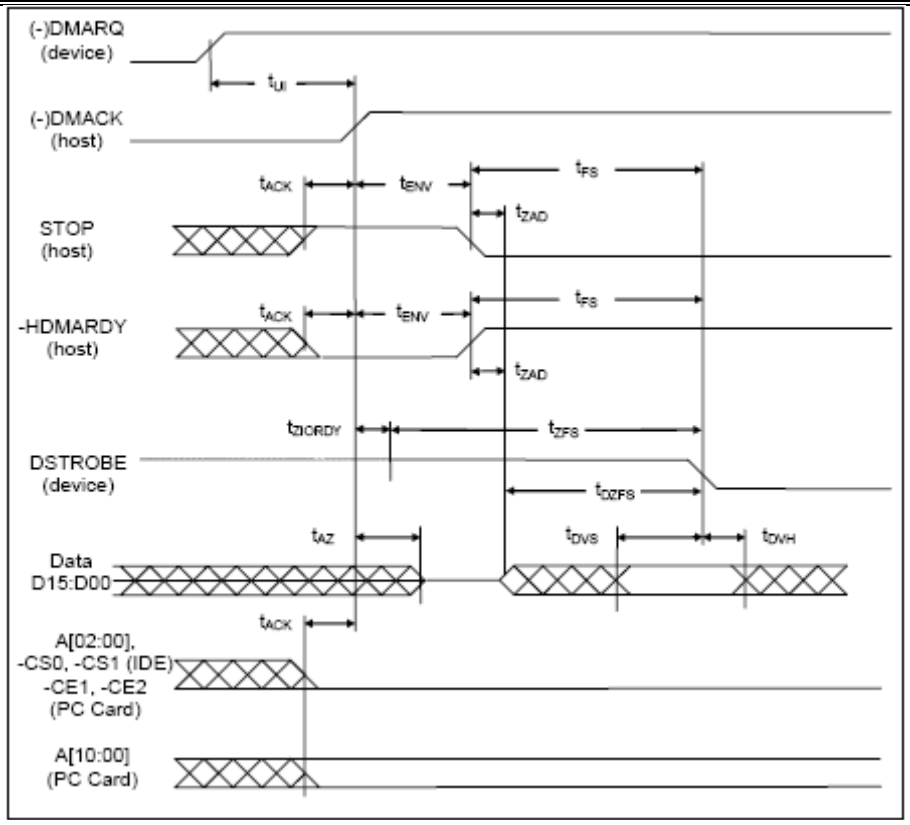

Figure 33: Ultra DMA Data-In Burst Initiation Timing

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes:
The definitions for the IORDY:-DDMARDY:DSTROBE, -IORD: -HDMARDY:HSTROBE, and -IOWR:STOP signal lines are not in effect until DMARQ and -DMACK are asserted. A[02:00], -CS0 & -CS1 are True IDE mode signal definitions. A[10:00], -CE1 and –CE2 are PC Card mode signals. The Bus polarity of (-)DMACK and (-)DMARQ are dependent on interface mode active.

6.19 Sustaining an Ultra DMA Data-In Burst

An Ultra DMA Data-In burst is sustained by following the steps lettered below. The timing diagram is shown in Figure 34: Sustained Ultra DMA Data-In Burst Timing. The timing parameters are specified in Table 23: Ultra DMA Data Burst Timing Requirements and are described in Table 24: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The device shall drive a data word onto D[15:00].

b) The device shall generate a DSTROBE edge to latch the new word no sooner than tDVS after changing the state of D[15:00]. The device shall generate a DSTROBE edge no more frequently than tCYC for the selected Ultra DMA mode. The device shall not generate two rising or two falling DSTROBE edges more frequently than 2tcyc for the selected Ultra DMA mode.

c) The device shall not change the state of D[15:00] until at least tDVH after generating a DSTROBE edge to latch the data.

d) The device shall repeat steps (a), (b), and (c) until the data transfer is complete or an Ultra DMA burst is paused, whichever occurs first.

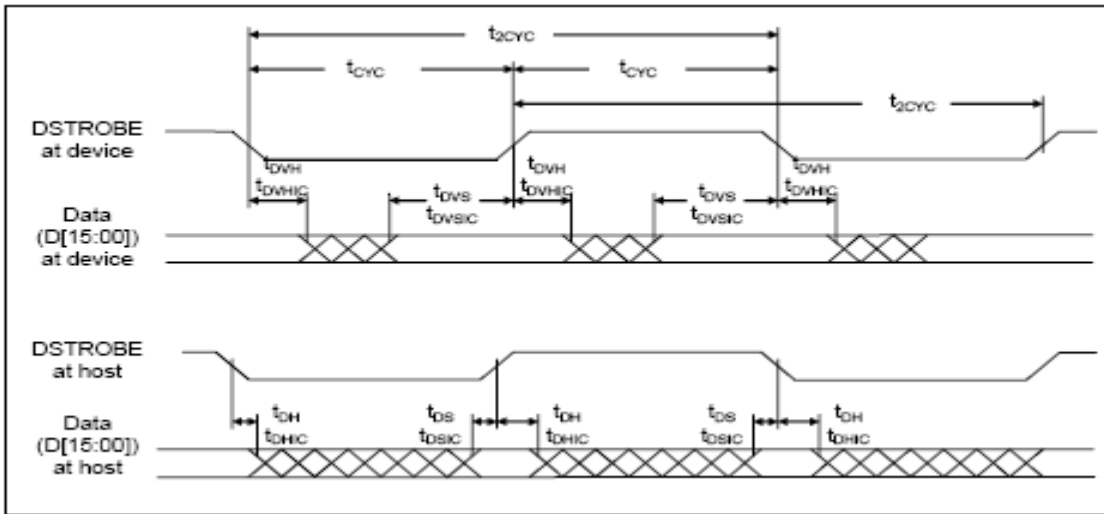

Figure 34: Sustained Ultra DMA Data-In Burst Timing

Notes: D[15:00] and DSTROBE signals are shown at both the host and the device to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the host until some time after they are driven by the device.

6.20 Host Pausing an Ultra DMA Data-In Burst

The host pauses a Data-In burst by following the steps lettered below. A timing diagram is shown in Figure 35: Ultra DMA Data-In Burst Host Pause Timing. The timing parameters are specified in Table 23: Ultra DMA Data Burst Timing Requirements and are described in Table 24: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The host shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.

b) The host shall pause an Ultra DMA burst by negating -HDMARDY.

c) The device shall stop generating DSTROBE edges within tRFS of the host negating -HDMARDY.

d) While operating in Ultra DMA modes 2, 1, or 0 the host shall be prepared to receive zero, one or two additional data words after negating -HDMARDY. While operating in Ultra DMA modes 6, 5, 4 or 3 the host shall be prepared to receive zero, one, two or three additional data words. The additional data words are a result of cable round trip delay and tRFS timing for the device.

e) The host shall resume an Ultra DMA burst by asserting -HDMARDY.

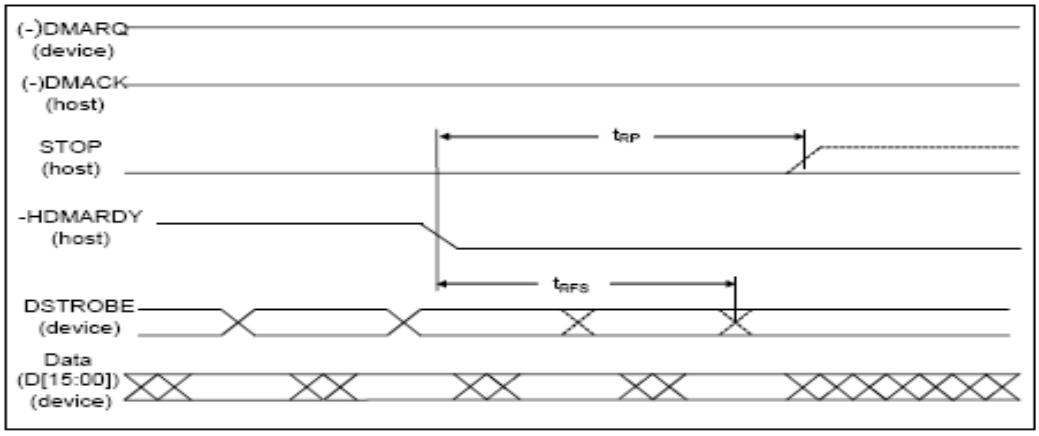

Figure 35: Ultra DMA Data-In Burst Host Pause Timing

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes:

1) The host may assert STOP to request termination of the Ultra DMA burst no sooner than tRP after -HDMARDY is negated.

2) After negating -HDMARDY, the host may receive zero, one, two, or three more data words from the device.

3) The bus polarity of the (-) DMARQ and (-)DMACK signals is dependent on the active interface mode.

6.21 Device Terminating an Ultra DMA Data-In Burst

The device terminates an Ultra DMA Data-In burst by following the steps lettered below. The timing diagram is shown in Figure 36: Ultra DMA Data-In Burst Device Termination Timing. The timing parameters are specified in Table 23: Ultra DMA Data Burst Timing Requirements and are described in Table 24: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The device shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred

b) The device shall pause an Ultra DMA burst by not generating DSTROBE edges.

c) NOTE The host shall not immediately assert STOP to initiate Ultra DMA burst termination when the device stops generating STROBE edges. If the device does not negate DMARQ, in order to initiate ULTRA DMA burst termination, the host shall negate -HDMARDY and wait tRP before asserting STOP.

d) The device shall resume an Ultra DMA burst by generating a DSTROBE edge.

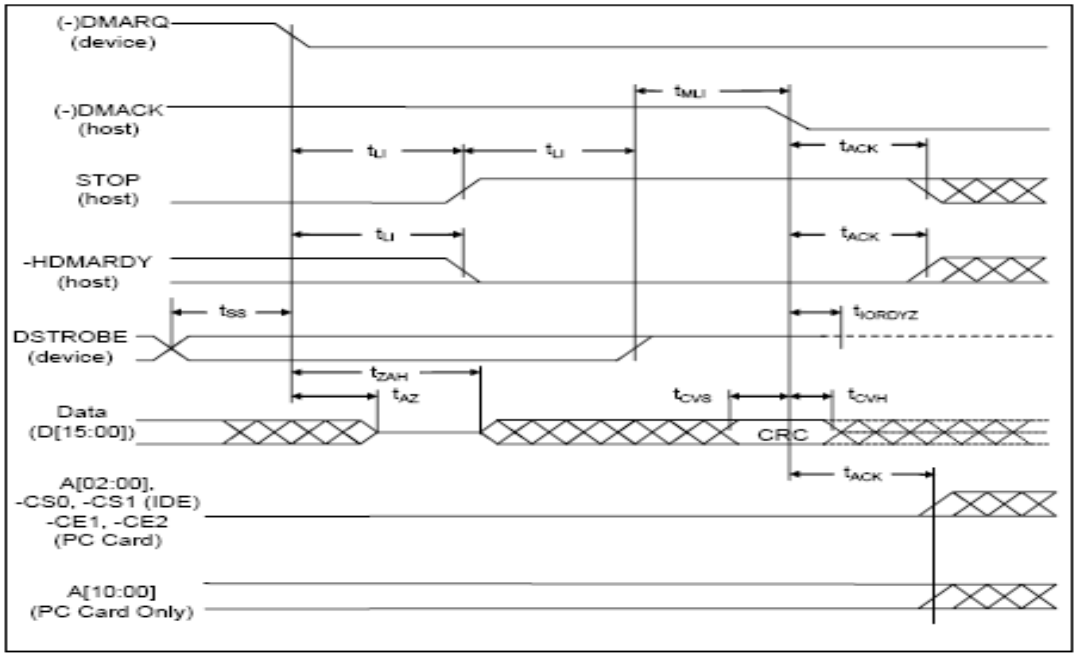

Figure 36: Ultra DMA Data-In Burst Device Termination Timing

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes:
The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated. A[02:00], -CS0 & -CS1 are True IDE mode signal definitions. A[10:00], -CE1 and –CE2 are PC Card mode signals. The bus polarity of DMARQ and DMACK are dependent on the active interface mode.

6.22 Host Terminating an Ultra DMA Data-In Burst

The host terminates an Ultra DMA Data-In burst by following the steps lettered below. The timing diagram is shown in Figure 37: Ultra DMA Data-In Burst Host Termination Timing. The timing parameters are specified in Table 23: Ultra DMA Data Burst Timing Requirements and are described in Table 24: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The host shall not initiate Ultra DMA burst termination until at least one data word of an Ultra DMA burst has been transferred.

b) The host shall initiate Ultra DMA burst termination by negating -HDMARDY. The host shall continue to negate -HDMARDY until the Ultra DMA burst is terminated.

c) The device shall stop generating DSTROBE edges within tRFS of the host negating -HDMARDY

d) While operating in Ultra DMA modes 2, 1, or 0 the host shall be prepared to receive zero, one or two additional data words after negating -HDMARDY. While operating in Ultra DMA modes 6, 5, 4 or 3 the host shall be prepared to receive zero, one, two or three additional data words. The additional data words are a result of cable round trip delay and tRFS timing for the device.

e) The host shall assert STOP no sooner than tRP after negating -HDMARDY. The host shall not negate STOP again until after the Ultra DMA burst is terminated.

f) The device shall negate DMARQ within tLI after the host has asserted STOP. The device shall not assert DMARQ again until after the Ultra DMA burst is terminated.

g) If DSTROBE is negated, the device shall assert DSTROBE within tLI after the host has asserted STOP. No data shall be transferred during this assertion. The host shall ignore this transition on DSTROBE. DSTROBE shall remain asserted until the Ultra DMA burst is terminated.

h) The device shall release D[15:00] no later than t AZ after negating DMARQ.

i) The host shall drive D[15:00] no sooner than tZAH after the device has negated DMARQ. For this step, the host may first drive D[15:00] with the result of its CRC calculation (see 4.3.18.6 Ultra DMA CRC Calculation).

j) If the host has not placed the result of its CRC calculation on D[15:00] since first driving D[15:00] during (9), the host shall place the result of its CRC calculation on D[15:00] (see 4.3.18.6 Ultra DMA CRC Calculation).

k) The host shall negate -DMACK no sooner than tMLI after the device has asserted DSTROBE and negated DMARQ and the host has asserted STOP and negated -HDMARDY, and no sooner than tDVS after the host places the result of its CRC calculation on D[15:00].

l) The device shall latch the host's CRC data from D[15:00] on the negating edge of -DMACK.

m) The device shall compare the CRC data received from the host with the results of its own CRC calculation. If a miscompare error occurs during one or more Ultra DMA burst for any one command, at the end of the command, the device shall report the first error that occurred (see 4.3.18.6 Ultra DMA CRC Calculation.

n) The device shall release DSTROBE within tIORDYZ after the host negates -DMACK.

o) The host shall neither negate STOP nor assert -HDMARDY until at least tACK after the host has negated -DMACK.

p) The host shall not assert -IORD, -CS0, -CS1, nor A[02:00] in True IDE mode (nor assert -IORD, -CE1, or –CE2, nor change A[10:00] in PC Card modes) until at least tACK after negating DMACK

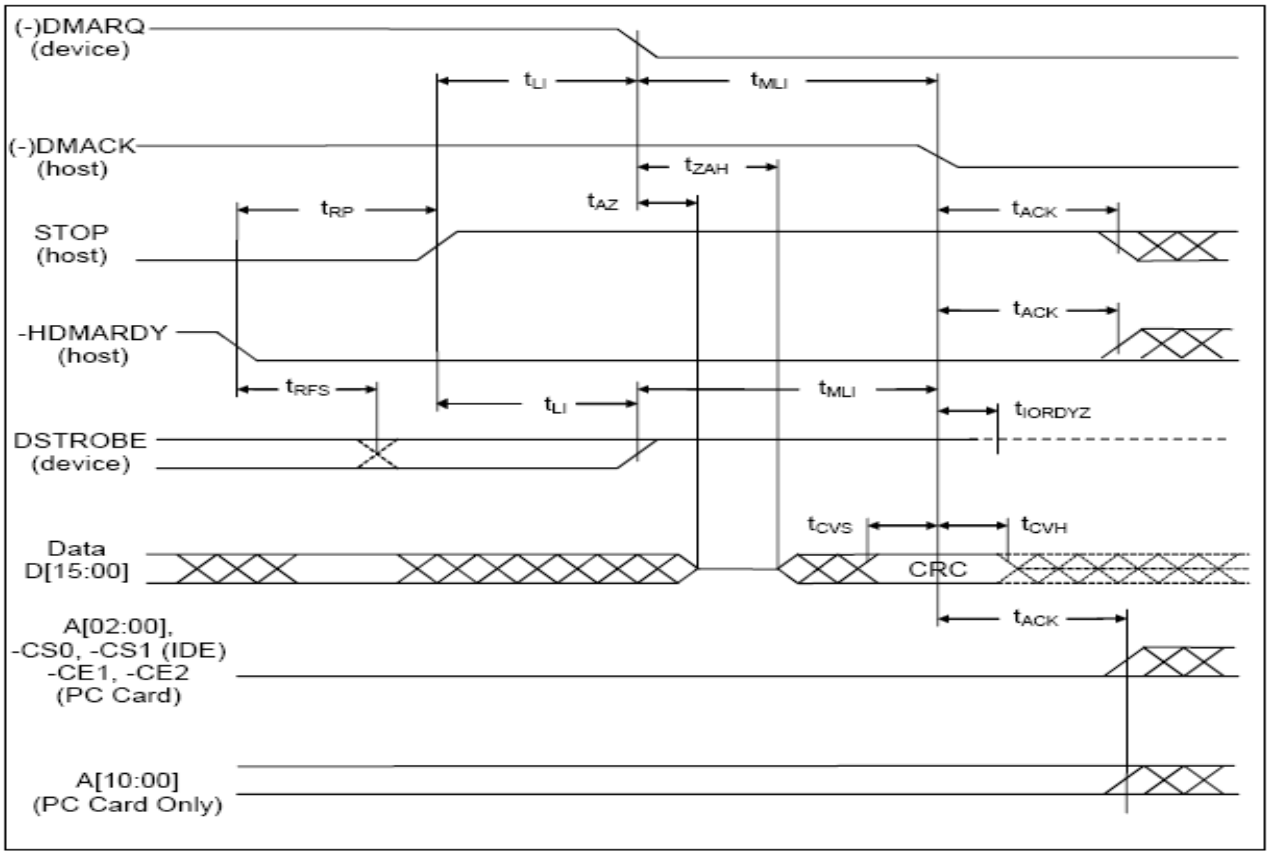

Figure 37: Ultra DMA Data-In Burst Host Termination Timing

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes:
The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated. A[02:00], -CS0 & -CS1 are True IDE mode signal definitions. A[10:00], -CE1 and –CE2 are PC Card mode signals. The bus polarity of DMARQ and DMACK depend on the active interface mode.

6.23 Initiating an Ultra DMA Data-Out Burst

An Ultra DMA Data-out burst is initiated by following the steps lettered below. The timing diagram is shown in Figure 38: Ultra DMA Data-Out Burst Initiation Timing. The timing parameters are specified in Table 23: Ultra DMA Data Burst Timing Requirements and are described in Table 24: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The host shall keep -DMACK in the negated state before an Ultra DMA burst is initiated.

b) The device shall assert DMARQ to initiate an Ultra DMA burst. c) Steps

(c), (d), and (e) may occur in any order or at the same time. The host shall assert STOP.

d) The host shall assert HSTROBE.

e) The host shall negate -CS0, -CS1, and A[02:00] in True IDE mode (or negate –CE1, -CE2 and hold A[10:0] fixed in PC Card modes). The host shall keep -CS0, -CS1, and A[02:00] negated in True IDE mode (or hold –CE1 and -CE2 negated and hold A[10:0] fixed in PC Card modes) until after negating -DMACK at the end of the burst.

f) Steps (c), (d), and (e) shall have occurred at least tACK before the host asserts -DMACK. The host shall keep -DMACK asserted until the end of an Ultra DMA burst.

g) The device may negate -DDMARDY tZIORDY after the host has asserted -DMACK. Once the device has negated -DDMARDY, the device shall not release -DDMARDY until after the host has negated DMACK at the end of an Ultra DMA burst.

h) The host shall negate STOP within tENV after asserting -DMACK. The host shall not assert STOP until after the first negation of HSTROBE.

i) The device shall assert -DDMARDY within tLI after the host has negated STOP. After asserting DMARQ and -DDMARDY the device shall not negate either signal until after the first negation of HSTROBE by the host.

j) The host shall drive the first word of the data transfer onto D[15:00]. This step may occur any time during Ultra DMA burst initiation.

k) To transfer the first word of data: the host shall negate HSTROBE no sooner than tUI after the device has asserted -DDMARDY. The host shall negate HSTROBE no sooner than tDVS after the driving the first word of data onto D[15:00].

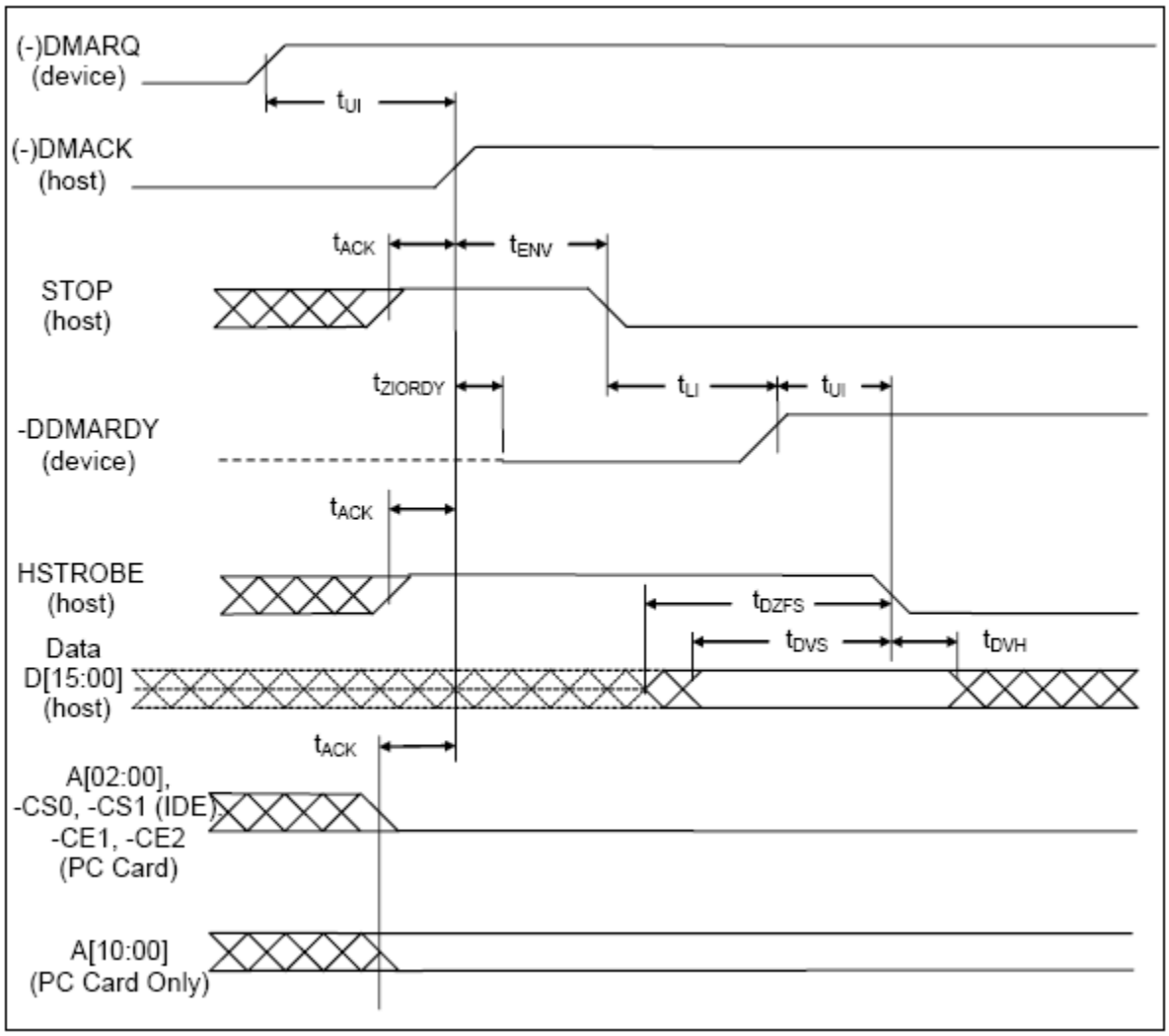

Figure 38: Ultra DMA Data-Out Burst Initiation Timing

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Note:
The definitions for the STOP, DDMARDY, and HSTROBE signal lines are not in effect until DMARQ and DMACK are asserted. A[02:00], -CS0 & -CS1 are True IDE mode signal definitions. A[10:00], -CE1 and –CE2 are PC Card mode signals. The bus polarity of DMARQ and DMACK depend on the active interface mode.

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6.24 Sustaining an Ultra DMA Data-Out Burst

An Ultra DMA Data-Out burst is sustained by following the steps lettered below. The timing diagram is shown in Figure 39: Sustained Ultra DMA Data-Out Burst Timing. The associated timing parameters are specified in Table 23: Ultra DMA Data Burst Timing Requirements and are described in Table 24: Ultra DMA Data Burst Timing Descriptions. The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The host shall drive a data word onto D[15:00].

b) The host shall generate an HSTROBE edge to latch the new word no sooner than tDVS after changing the state of D[15:00]. The host shall generate an HSTROBE edge no more frequently than tCYC for the selected Ultra DMA mode. The host shall not generate two rising or falling HSTROBE edges more frequently than 2tcyc for the selected Ultra DMA mode.

c) The host shall not change the state of D[15:00] until at least tDVH after generating an HSTROBE edge to latch the data.

d) The host shall repeat steps (a), (b), and (c) until the data transfer is complete or an Ultra DMA burst is paused, whichever occurs first.

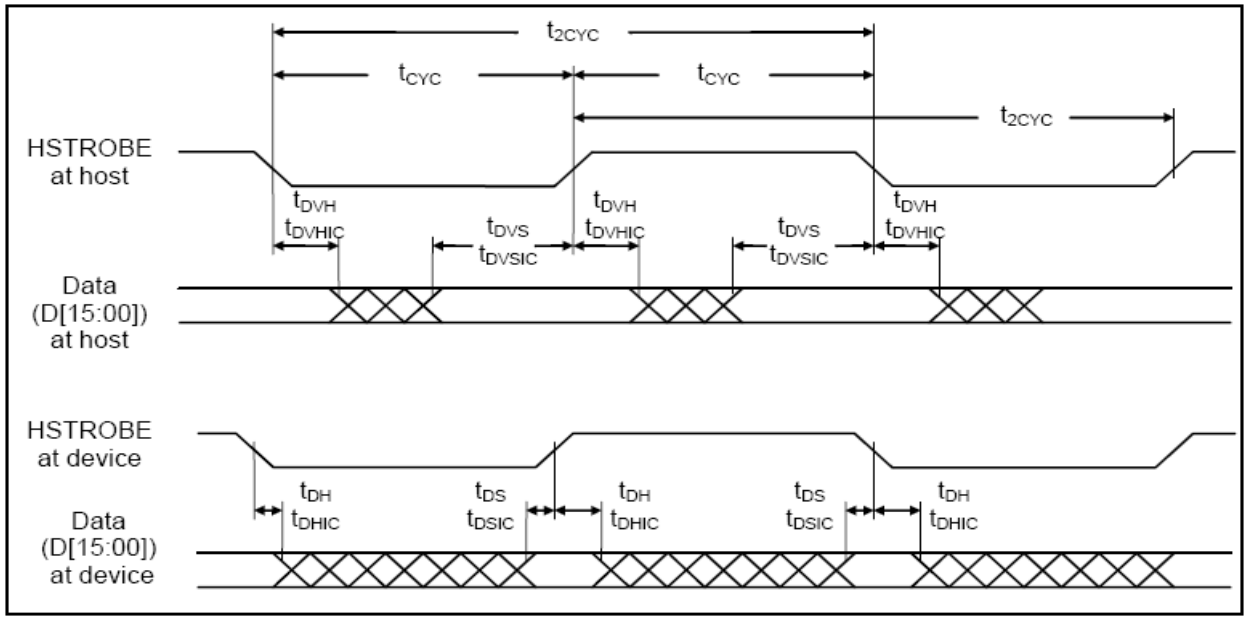

Figure 39: Sustained Ultra DMA Data-Out Burst Timing

Note:
Data (D[15:00]) and HSTROBE signals are shown at both the device and the host to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the device until some time after they are driven by the host.

6.25 Device Pausing an Ultra DMA Data-Out Burst

The device pauses an Ultra DMA Data-Out burst by following the steps lettered below. The timing diagram is shown in Figure 40: Ultra DMA Data-Out Burst Device Pause Timing. The timing parameters are specified in Table 23: Ultra DMA Data Burst Timing Requirements and are described in Table 24: Ultra DMA Data Burst Timing Descriptions. The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The device shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.

b) The device shall pause an Ultra DMA burst by negating -DDMARDY.

c) The host shall stop generating HSTROBE edges within tRFS of the device negating -DDMARDY.

d) While operating in Ultra DMA modes 2, 1, or 0 the device shall be prepared to receive zero, one or two additional data words after negating -HDMARDY. While operating in Ultra DMA modes 6, 5, 4 or 3 the device shall be prepared to receive zero, one, two or three additional data words. The additional data words are a result of cable round trip delay and tRFS timing for the device.

e) The device shall resume an Ultra DMA burst by asserting -DDMARDY.

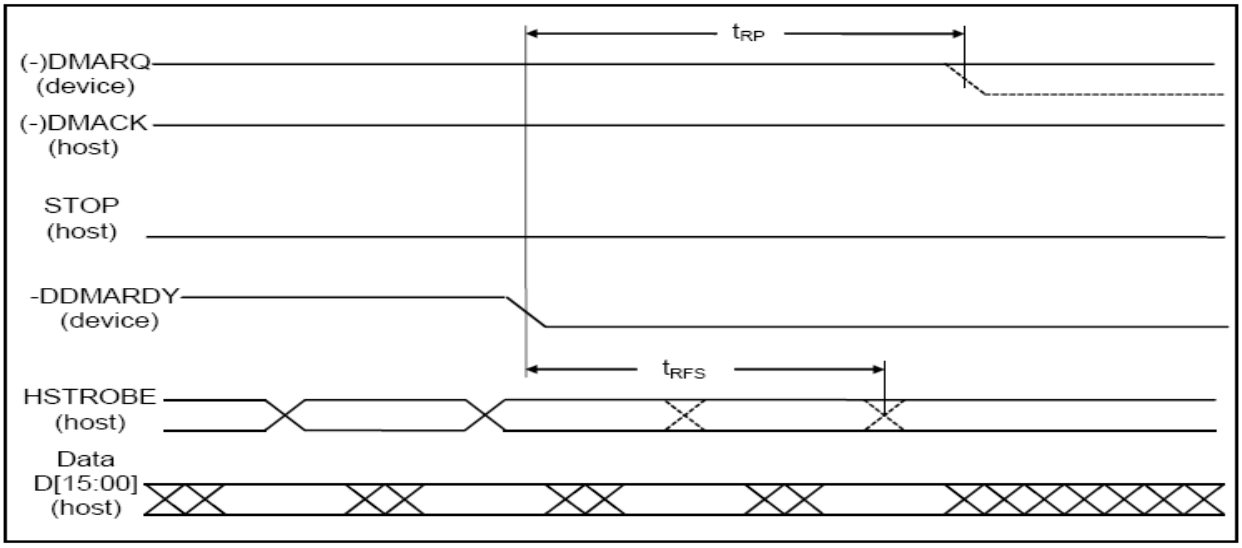

Figure 40: Ultra DMA Data-Out Burst Device Pause Timing

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes:

1) The device may negate DMARQ to request termination of the Ultra DMA burst no sooner than tRP after -DDMARDY is negated.

2) After negating -DDMARDY, the device may receive zero, one, two, or three more data words from the host.

3) The bus polarity of DMARQ and DMACK depend on the active interface mode.

6.26 Device Terminating an Ultra DMA Data-Out Burst

The device terminates an Ultra DMA Data-Out burst by following the steps lettered below. The timing diagram for the operation is shown in Figure 41: Ultra DMA Data-Out Burst Device Termination Timing. The timing parameters are specified in Table 23: Ultra DMA Data Burst Timing Requirements and are described in Table 24: Ultra DMA Data Burst Timing Descriptions. The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The device shall not initiate Ultra DMA burst termination until at least one data word of an Ultra DMA burst has been transferred.

b) The device shall initiate Ultra DMA burst termination by negating -DDMARDY.

c) The host shall stop generating an HSTROBE edges within tRFS of the device negating -DDMARDY.

d) While operating in Ultra DMA modes 2, 1, or 0 the device shall be prepared to receive zero, one or two additional data words after negating -HDMARDY. While operating in Ultra DMA modes 6, 5, 4 or 3 the device shall be prepared to receive zero, one, two or three additional data words. The additional data words are a result of cable round trip delay and tRFS timing for the device.

e) The device shall negate DMARQ no sooner than tRP after negating -DDMARDY. The device shall not assert DMARQ again until after the Ultra DMA burst is terminated.

f) The host shall assert STOP within tLI after the device has negated DMARQ. The host shall not negate STOP again until after the Ultra DMA burst is terminated.

g) If HSTROBE is negated, the host shall assert HSTROBE within tLI after the device has negated DMARQ. No data shall be transferred during this assertion. The device shall ignore this transition of HSTROBE. HSTROBE shall remain asserted until the Ultra DMA burst is terminated.

h) The host shall place the result of its CRC calculation on D[15:00] (see 4.3.18.6 Ultra DMA CRC Calculation).

i) The host shall negate -DMACK no sooner than tMLI after the host has asserted HSTROBE and STOP and the device has negated DMARQ and -DDMARDY, and no sooner than tDVS after placing the result of its CRC calculation on D[15:00].

j) The device shall latch the host's CRC data from D[15:00] on the negating edge of -DMACK.

k) The device shall compare the CRC data received from the host with the results of its own CRC calculation. If a miscompare error occurs during one or more Ultra DMA bursts for any one command, the device shall report the first error that occurred (see 4.3.18.6 Ultra DMA CRC Calculation).

l) The device shall release DSTROBE within tIORDYZ after the host negates –DMACK.

m) The host shall not negate STOP nor assert –HDMARDY until at least tACK after negating –DMACK.

n) The host shall not assert –IORD, -CS0, -CS1, -CE1, -CE2 or change addresses until at least tACK after negating DMACK.

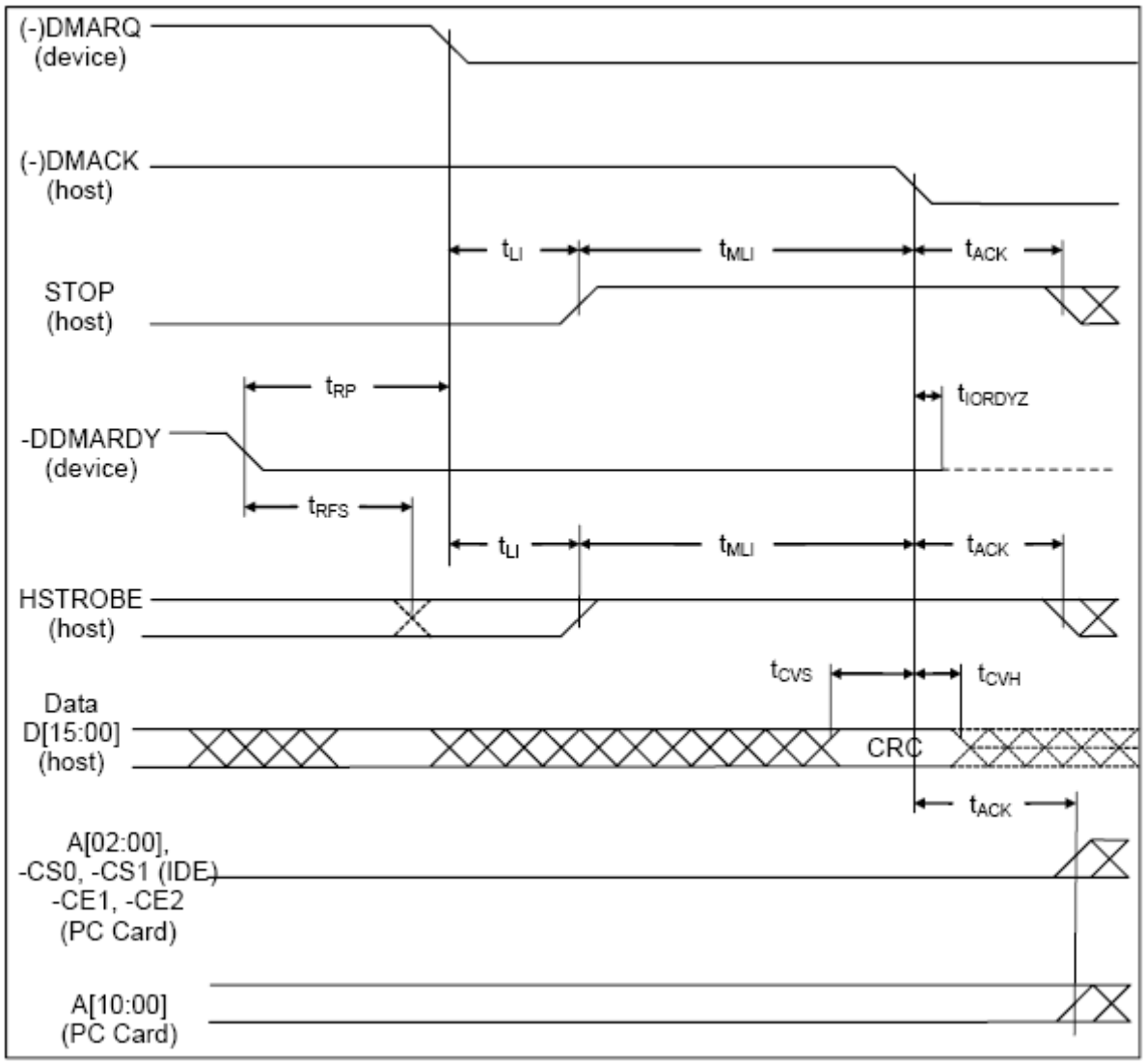

Figure 41: Ultra DMA Data-Out Burst Device Termination Timing

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Note:
The definitions for the STOP, DDMARDY, and HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated. A00-A02, -CS0 & -CS1 are True IDE mode signal definitions. A00-A10, -CE1 and –CE2 are PC Card mode signals. The bus polarity of DMARQ and DMACK depend on the active interface mode.

6.27 Host Terminating an Ultra DMA Data-Out Burst

Termination of an Ultra DMA Data-Out burst by the host is shown in Figure 42: Ultra DMA Data-Out Burst Host Termination Timing while timing parameters are specified in Table 23: Ultra DMA Data Burst Timing Requirements and timing parameters are described in Table 24: Ultra DMA Data Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The host shall initiate termination of an Ultra DMA burst by not generating HSTROBE edges.

b) The host shall assert STOP no sooner than tSS after it last generated an HSTROBE edge. The host shall not negate STOP again until after the Ultra DMA burst is terminated.

c) The device shall negate DMARQ within tLI after the host asserts STOP. The device shall not assert DMARQ again until after the Ultra DMA burst is terminated.

d) The device shall negate -DDMARDY within tLI after the host has negated STOP. The device shall not assert -DDMARDY again until after the Ultra DMA burst termination is complete.

e) If HSTROBE is negated, the host shall assert HSTROBE within tLI after the device has negated DMARQ. No data shall be transferred during this assertion. The device shall ignore this transition on HSTROBE. HSTROBE shall remain asserted until the Ultra DMA burst is terminated.

f) The host shall place the result of its CRC calculation on D[15:00] (see 4.3.18.6 Ultra DMA CRC Calculation).

g) The host shall negate -DMACK no sooner than tMLI after the host has asserted HSTROBE and STOP and the device has negated DMARQ and -DDMARDY, and no sooner than tDVS after placing the result of its CRC calculation on D[15:00].

h) The device shall latch the host's CRC data from D[15:00] on the negating edge of -DMACK.

i) The device shall compare the CRC data received from the host with the results of its own CRC calculation. If a miscompare error occurs during one or more Ultra DMA bursts for any one command, at the end of the command, the device shall report the first error that occurred (see 4.3.18.6 Ultra DMA CRC Calculation).

j) The device shall release -DDMARDY within t IORDYZ after the host has negated -DMACK.

k) The host shall neither negate STOP nor negate HSTROBE until at least tACK after negating -DMACK.

l) The host shall not assert -IOWR, -CS0, -CS1, The host shall not assert –IORD, -CS0, -CS1, -CE1, -CE2 or change A[10:00] until at least tACK after negating DMACK.

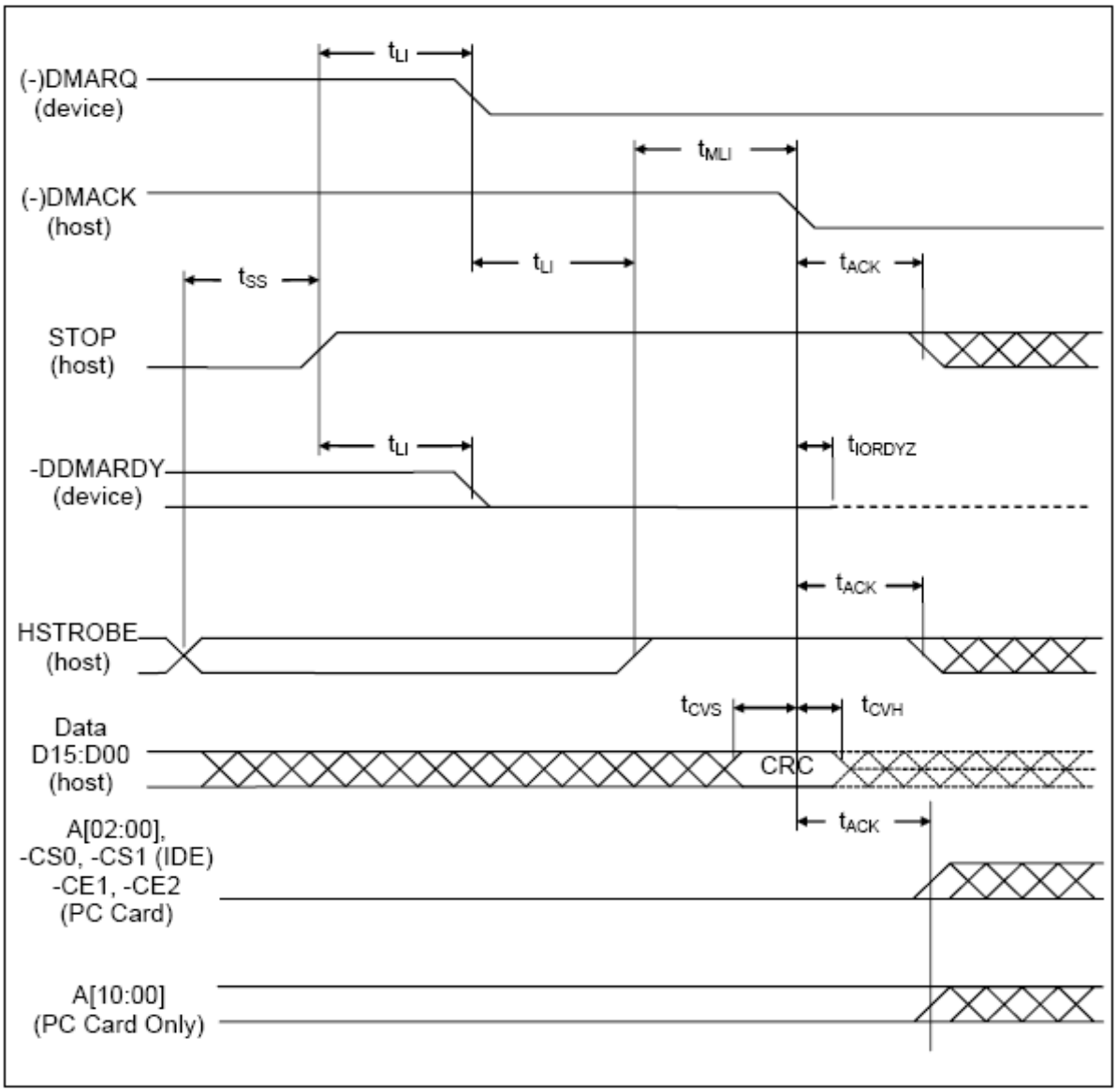

Figure 42: Ultra DMA Data-Out Burst Host Termination Timing

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes:
The definitions for the STOP, DDMARDY, and HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated. A[02:00], -CS0 & -CS1 are True IDE mode signal definitions. A[10:00], -CE1 and –CE2 are PC Card mode signals. The bus polarity of DMARQ and DMACK depend on the active interface mode.

6.28 HUltra DMA CRC Calculation

The following is a list of rules for calculating CRC, determining if a CRC error has occurred during an Ultra DMA burst, and reporting any error that occurs at the end of a command.

1. Both the host and the device shall have a 16-bit CRC calculation function.
2. Both the host and the device shall calculate a CRC value for each Ultra DMA burst.

3. The CRC function in the host and the device shall be initialized with a seed of 4ABAh at the beginning of an Ultra DMA burst before any data is transferred.

4. For each STROBE transition used for data transfer, both the host and the device shall calculate a new CRC value by applying the CRC polynomial to the current value of their individual CRC functions and the word being transferred. CRC is not calculated for the return of STROBE to the asserted state after the Ultra DMA burst termination request has been acknowledged.

5. At the end of any Ultra DMA burst the host shall send the results of its CRC calculation function to the device on D[15:00] with the negation of -DMACK.

6. The device shall then compare the CRC data from the host with the calculated value in its own CRC calculation function. If the two values do not match, the device shall save the error and report it at the end of the command. A subsequent Ultra DMA burst for the same command that does not have a CRC error shall not clear an error saved from a previous Ultra DMA burst in the same command. If a miscompare error occurs during one or more Ultra DMA bursts for any one command, at the end of the command, the device shall report the first error that occurred.

7. For READ DMA, WRITE DMA, READ DMA QUEUED, or WRITE DMA QUEUED commands: When a CRC error is detected, it shall be reported by setting both ICRC and ABRT (bit 7 and bit 2 in the Error register) to one. ICRC is defined as the “Interface CRC Error” bit. The host shall respond to this error by re-issuing the command.

8. For a REQUEST SENSE packet command (see SPC T10/955D for definition of the REQUEST SENSE command): When a CRC error is detected during transmission of sense data the device shall complete the command and set CHK to one. The device shall report a Sense key of 0Bh (ABORTED COMMAND). The device shall preserve the original sense data that was being returned when the CRC error occurred. The device shall not report any additional sense data specific to the CRC error. The host device driver may retry the REQUEST SENSE command or may consider this an unrecoverable error and retry the command that caused the Check Condition.

9. For any packet command except a REQUEST SENSE command: If a CRC error is detected, the device shall complete the command with CHK set to one. The device shall report a Sense key of 04h (HARDWARE ERROR). The sense data supplied via a subsequent REQUEST SENSE command shall report an ASC/ASCQ value of 08h/03h (LOGICAL UNIT COMMUNICATION CRC ERROR). Host drivers should retry the command that resulted in a HARDWARE ERROR. NOTE If excessive CRC errors are encountered while operating in Ultra mode 2 or 1, the host should select a slower Ultra mode. Caution: CRC errors are detected and reported only while operating in an Ultra mode.

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10. A host may send extra data words on the last Ultra DMA burst of a data out command. If a device determines that all data has been transferred for a command, the device shall terminate the burst. A device may have already received more data words than were required for the command. These extra words are used by both the host and the device to calculate the CRC, but, on an Ultra DMA data out burst, the extra words shall be discarded by the device.

11. The CRC generator polynomial is: G(X) = X16 + X12 + X5 + 1. Table 28 describes the equations for 16-bit parallel generation of the resulting polynomial (based on a word boundary).

NOTE Since no bit clock is available, the recommended approach for calculating CRC is to use a word clock derived from the bus strobe. The combinational logic is then equivalent to shifting sixteen bits serially through the generator polynomial where D00 is shifted in first and D15 is shifted in last.

Table 27: Equations for parallel generation of an Ultra DMA CRC

CRCIN0 = f16	CRCIN8 = f8 XOR f13
CRCIN1 = f15	CRCIN9 = f7 XOR f12
CRCIN2 = f14	CRCIN10 = f6 XOR f11
CRCIN3 = f13	CRCIN11 = f5 XOR f10
CRCIN4 = f12	CRCIN12 = f4 XOR f9 XOR f16
CRCIN5 = f11 XOR f16	CRCIN13 = f3 XOR f8 XOR f15
CRCIN6 = f10 XOR f15	CRCIN14 = f2 XOR f7 XOR f14
CRCIN7 = f9 XOR f14	CRCIN15 = f1 XOR f6 XOR f13
f1 = D00 XOR CRCOUT15	f9 = D08 XOR CRCOUT7 XOR f5
f2 = D01 XOR CRCOUT14	f10 = D09 XOR CRCOUT6 XOR f6
f3 = D02 XOR CRCOUT13	f11 = D10 XOR CRCOUT5 XOR f7
f4 = D03 XOR CRCOUT12	f12 = D11 XOR CRCOUT4 XOR f1 XOR f8
f5 = D04 XOR CRCOUT11 XOR f1	f13 = D12 XOR CRCOUT3 XOR f2 XOR f9
f6 = D05 XOR CRCOUT10 XOR f2	f14 = D13 XOR CRCOUT2 XOR f3 XOR f10
f7 = D06 XOR CRCOUT9 XOR f3	f15 = D14 XOR CRCOUT1 XOR f4 XOR f11
f8 = D07 XOR CRCOUT8 XOR f4	f16 = D15 XOR CRCOUT0 XOR f5 XOR f12

Notes:

1) f=feedback

2) D[15:0] = Data to or from the bus

3) CRCOUT = 16-bit edge triggered result (current CRC)

4) CRCOUT[15:0] are sent on matching order bits of D[15:00]

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
V_{CC}	Input Power	-0.3 ~ 6.0	V
T_{STG}	Storage Temperature	-65 ~ 150	˚C
I_{OP}	Operating Current	60	mA
I_{STB}	Standby Current	6	mA

7.2 Recommended Operating Conditions

Symbol	Parameter		Ratings	Unit
V_{CC}	Input Power	5V	4.5 to 5.5	V
		3.3V	3.13 to 3.47	V
T_A	Operating Temperature	Commercial	0 to 70	˚C
		Industrial	-40 to 85	˚C

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7.3 DC Electrical Characteristics

(T_A = 0 to 70˚C V_{DD} = 3.3V +/-5%)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage	CMOS		2.4			V
V_{IL}	Low Level Input Voltage	CMOS				0.6	V
V_T	Switching Threshold	CMOS			1.8		V
V_{T+}	Switching Threshold, Positive Going Threshold	CMOS				2.0	V
V_{T-}	Switching Threshold, Negative Going Threshold	CMOS		1.0			V
I_{IH}	High Level Input Current	Input Buffer	$V_{IN} = V_{DD}$	-10		10	uA
		Input Buffer with pull-up		-160	-30	-10	uA
I_{IL}	Low Level Input Current	Input Buffer	$V_{IN} = V_{SS}$	-10		10	uA
		Input Buffer with pull-up		-160	-30	-10	uA
V_{OH}	High Level Output Current			2.4			V
V_{OL}	Low Level Output Current					0.4	V
I_{OZ}	Tri-state Leakage Current		V_{OUT} =V_{SS} or V_{DD}	-10		10	uA
I_{DD}	Maximum Operating Current		V_{DD} = 303V		30	40	mA
I_{idle}	Idle Current		F_{CLK} = 20MHz			20	mA
I_{ds}	Stop Current					30	uA

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DC Electrical Characteristics (cont.)

(TA = 0 to 70˚C VDD = 5V +/-10%)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage	CMOS		3.5			V
V_{IL}	Low Level Input Voltage	CMOS				1.5	V
V_T	Switching Threshold	CMOS			2.5		V
V_{T+}	Switching Threshold, Positive Going Threshold	CMOS				4.0	V
V_{T-}	Switching Threshold, Negative Going Threshold	CMOS		1.0			V
I_{IH}	High Level Input Current	Input Buffer	$V_{IN} = V_{DD}$	-10		10	uA
		Input Buffer with pull-up		10	50	100	uA
I_{IL}	Low Level Input Current	Input Buffer	$V_{IN} = V_{SS}$	-10		10	uA
		Input Buffer with pull-up		-100	-50	-10	uA
V_{OH}	High Level Output Current			2.4			V
V_{OL}	Low Level Output Current					0.4	V
I_{OZ}	Tri-state Leakage Current		$V_{OUT} = V_{SS}$ or V_{DD}	-10		10	uA
I_{DD}	Maximum Operating Current		V_{DD} = 303V F_{CLK} = 20MHz		60	70	mA
I_{idle}	Idle Current					35	mA
I_{ds}	Stop Current					60	uA

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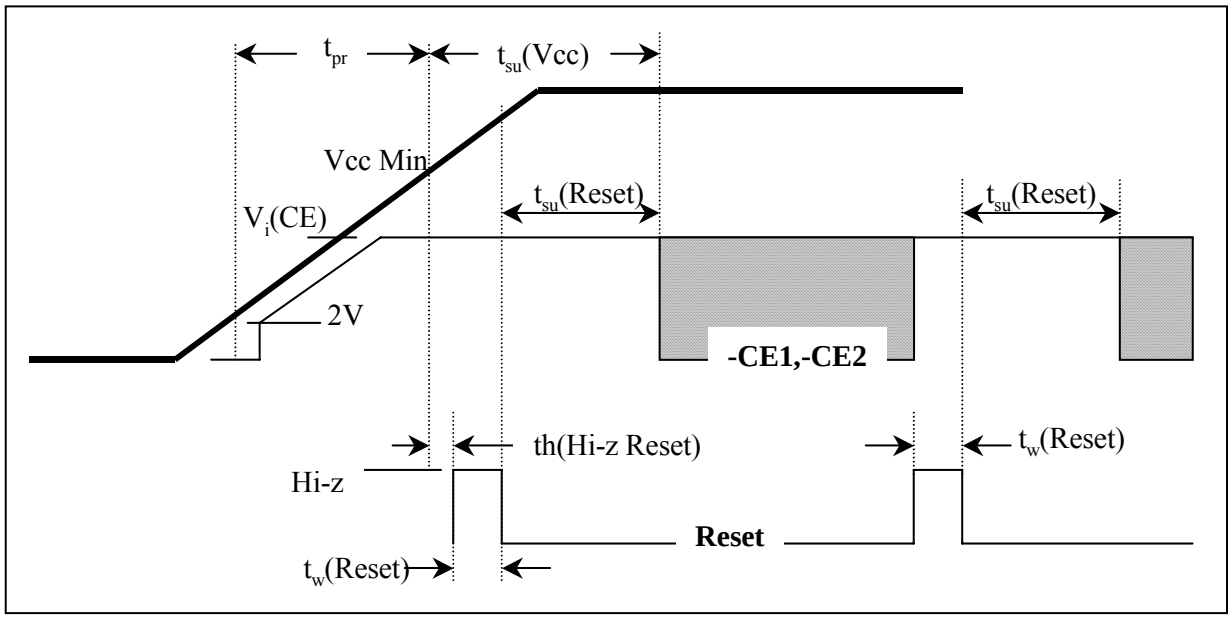
7.4 Power-up/Power-down Timing

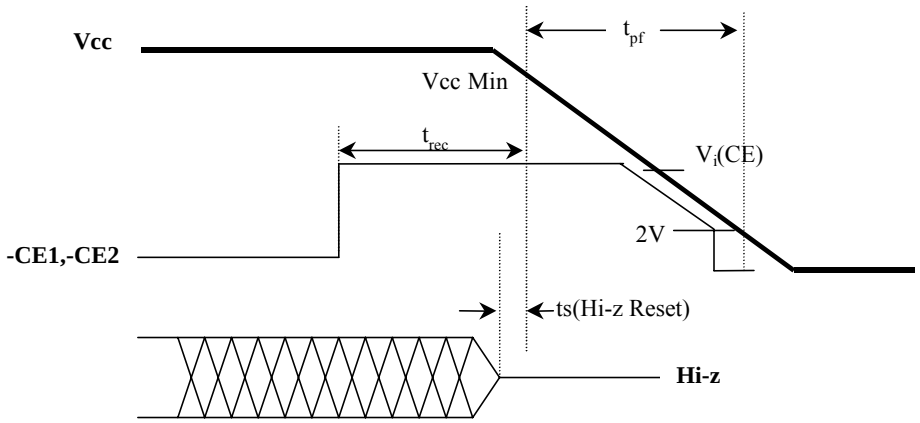
The following timing requirements are defined to permit the ATA controller to perform power-up initialization and to complete procedures prior to power down.

Item	Symbol	Condition	Value		
			Min	Max	Unit
Card Enable Signal Level[1]	Vi(CE)	0V ≤ Vcc < 2.0V	0	ViMAX	V
		2.0V ≤ Vcc < V_{IH}	Vcc-0.1	ViMAX	V
		V_{IH} ≤ Vcc	V_{IH}	ViMAX	V
Card Enable Setup Time	t_{su}(Vcc)		20		ms
RESET Setup Time	t_{su}(RESET)		20		ms
Card Enable Recover Time	t_{rec}(Vcc)		0.001		ms
Vcc Rising Time	t_{pr}	10% → 90% of Vcc	0.1	100	ms
Vcc Falling Time	t_{pf}	90% of Vcc → 10%	3.0	300	ms
RESET Width	t_w(RESET)		10		us
	t_h(Hi-z RESET)		1		ms
	t_s(Hi-z RESET)		0		ms

1. ViMAX means Absolute Maximum Voltage for Input in the period of 0V ≤ Vcc < 2.0V, Vi(CE) is only 0V ~ViMAX
2. The t_{pr} and t_{pf} are defined as "linear waveform" in the period of 10% to 90% or vice-versa. Even if the waveform is not "linear waveform", its rising and falling time must be met by this specification.



Power-Up / Power-Down Timing (cont.)



Power-Down Timing

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