



SMART
Embedded
Products

Product Specification

**SMART MODULAR
microSD™ MEMORY CARDS
128MB, 1GB and 2GB
SDSC Memory Cards
4GB SDHC Memory Cards**

March 2018
DSUD352-AC



www.smartm.com

REVISION HISTORY

Date	Revision	Section(s)	Description
May 2017	AA	All	Initial Release.
October 2017	AB	All	Added part number.
March 2018	AC	All	Added part number.



ESD Caution – Handling

Static electricity may be discharged through this disk subsystem. In extreme cases, this may temporarily interrupt the operation or damage components. To prevent this, make sure you are working in an ESD-safe environment. For example, before handling the disk subsystem, touch a grounded device, such as a computer case, prior to handling.

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1. GENERAL DESCRIPTION

1.1. Overview

SMART's microSD Memory Card product offering is specifically targeted at the needs of OEM markets such as networking, telecommunications and data communications. SMART's SD products are also a natural fit for mobile and embedded computing, medical, automotive and industrial applications.

SMART's microSD products offer reliable, high performance operation in an industry standard ultrasonic welded SD housing. They are available in 128MB to 4 GB capacities.

Incorporating on-board error detection and correction algorithms and static and dynamic wear leveling techniques insure SMART's microSD products provide years of reliable operation.

SMART has built its foundation by providing proven technology and quality products to the most demanding Fortune 100 OEMs. SMART engineers its products to perform at the highest degree of reliability & compatibility while backing these products with outstanding services and technology expertise.

About SMART

SMART is a leading independent manufacturer of memory and embedded modular subsystems inclusive of board-level through system-level design, manufacturing, test, and fulfillment services. We offer more than 500 standard and custom products to leading OEMs in the computer, industrial, networking and telecommunications industries worldwide.

1.2. Features

- **Form Factor:** microSD
- **Interface:** Industry standard SD [Part 1 Physical Layer Specification Ver3.01 Final]
- **Supports SD SPI Mode**
- **Bus Widths Supported:** x1 and x4
- **Supported Bus Speed Modes (using x4 bus width)**
 - **Non-UHS mode**
 - **Default Speed Mode:** 3.3 V signaling, up to 25 MHz, up to 12.5 MB/s
 - **High Speed Mode:** 3.3 V signaling, up to 50 MHz, up to 25 MB/s

NOTE: SDSC cards (capacity less than and including 2GB) support only non-UHS mode

➢ UHS-I mode

- **Default Speed Mode:** 3.3 V signaling, up to 25 MHz
- **High Speed Mode:** 3.3 V signaling, up to 50 MHz
- **SDR12:** 1.8 V signaling, up to 25 MHz SDR
- **SDR25:** 1.8 V signaling, up to 50 MHz SDR
- **SDR50:** 1.8 V signaling, up to 100 MHz SDR
- **SDR104:** 1.8 V signaling, up to 208 MHz SDR
- **DDR50:** 1.8 V signaling, up to 50 MHz DDR

NOTE: Timing varies between UHS-I (1.8 V) and Standard (3.3 V) signaling

- **NAND Technology:** Single Level Cell (SLC)
- **Capacity:**
 - SDSC: 128Mbytes, 1GBytes and 2GBytes
 - SDHC: 4GBytes
- **Operating Temperature:**
 - **Commercial:** 0°C to 70°C
 - **Extended:** -25°C to +85°C
 - **Industrial:** -40°C to +85°C
- **Input Power:** 2.7 V – 3.6 V
- **Dimensions:** 15 mm(L) x 11 mm(W) x 1 mm(H)
- **ESD protection:** +4 kV/-4 kV in contact pads

1.3. Unique Features

- Implements Static and Dynamic Wear Leveling for longer life
- Device health information (erase count, bad block and spare count) is available via vendor specific command (Application Note available upon request)
- Copyright Protection Mechanism: fully-compliant to the highest security SDMI Standard
- Supports CPRM (Content Protection for Recordable Media) for recorded content
- Password Protection of cards (optional)
- Built-in write protection features (permanent and temporary)
- RoHS compliant and Low Halogen
- Bus Speed Mode
 - 128MB, 1GB and 2GB: Non-UHS
 - 4GB: UHS-I

2. OPERATIONAL CHARACTERISTICS

All listed values are typical unless otherwise stated.

2.1. Performance

Table 1: Performance Characteristics (Sequential) ⁽¹⁾

Drive	Bus Configuration	Sequential Read	Sequential Write
128MB	High speed mode	22	3
1 GB		23	22
2 GB		23	22
4 GB	SDR104 mode	68	50

Note: ¹Performance measured using TestMetrix.

2.2. Operating Power Consumption

Table 2: Power Requirements

Drive	Standby Current (Max) µA	Write Current (Max) mA	Read Current (Max) mA
128MB	127	72	74
1 GB	140	200	149
2 GB	162	218	197
4 GB	198	213	217

2.3. Reliability

Table 3: Reliability Characteristics

Item	Value
Mean Time Between Failures (MTBF) (@ 25°C)	> 3 Million hours
Data Reliability	< 1 Non-Recoverable Error in 10 ¹⁴ bits read
Data Retention (@ 40°C)	10 years > 90% life remaining
	1 year < 10% life remaining
Endurance ¹	SLC: 6 TBytes per 1 GB card capacity
Error Correction / Error Detection	Up to 24 bits for every 1 Kbyte user data

¹ Endurance is directly related to the application specific workload

2.4. Endurance

- Static & Dynamic Wear Leveling:** This feature eliminates overstressing flash media by spreading the data writes across all flash physical address space, including logical areas that are not written by the user. The data is wear leveled across the entire drive.
- ECC:** microSD products utilize BCH ECC to provide correction of up to 24 random single-bit errors per 1 Kbyte block of user data.
- Bad Block Management:** This feature tracks all manufacturing and run-time bad blocks of flash media and replaces them with new ones from the spare pool.

2.5. Environmental Conditions

Table 4: Environmental Conditions and Test Conditions

Parameter	Value
Shock	Plus with Half-Sine, 500G/2ms. 6 faces, 5 times/face
Bending Test	Force: 10N, hold 1 min for 5 times
Vibration	Displacement: 20-80Hz/1.52mm Acceleration: 80-2000HZ/20G 30mins/axis
Temperature and Humidity storage	40°C/93%RH@500hrs
Operating Temperature - Commercial	0°C to +70°C
Operating Temperature - Extended	-25°C to +85°C
Operating Temperature - Industrial	-40°C to +85°C
Storage Temperature	-40°C to +85°C

2.6. Physical Characteristics

Table 5: Physical Characteristics

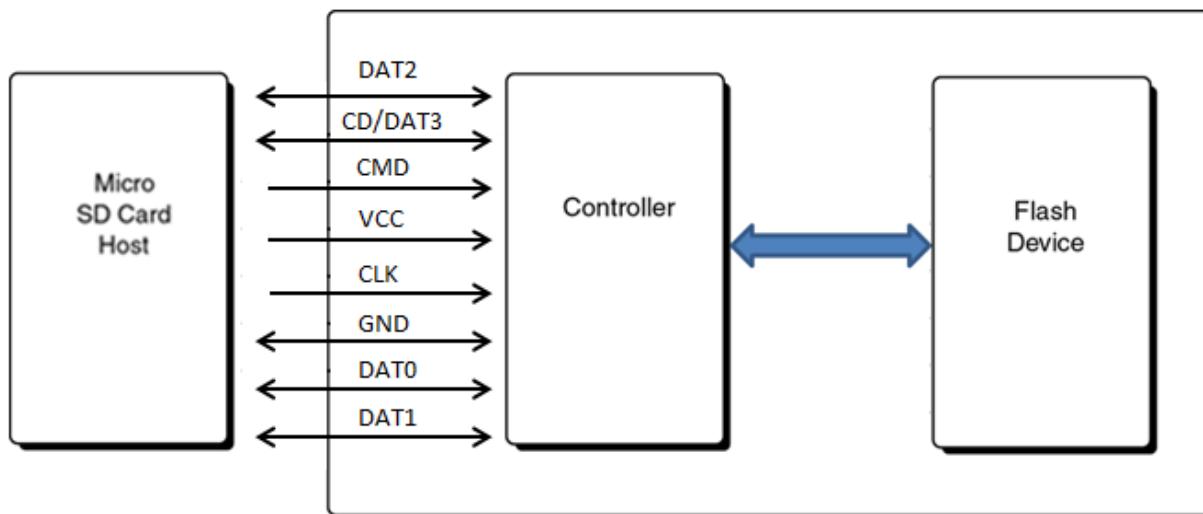
Parameter	Value
Length	15.0 mm [0.590 in]
Width	11.0 mm [0.433 in]
Thickness	1.0 mm [0.039 in]
Weight	0.4 g [0.014 oz]

3. PRODUCT DESCRIPTION

SMART's microSD Memory Card product line is offered in a UL approved housing with an advanced 8-pin connector. It contains a controller and a flash memory device. The on-board controller interfaces with a microSD Card Host allowing data to be written to and read from the flash memory device.

3.1. Functional Block Diagram

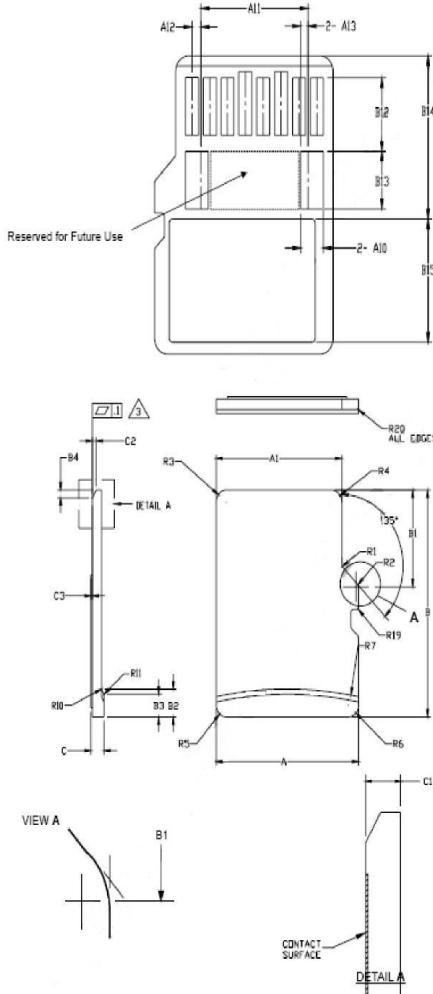
Figure 1: microSD Block Diagram



4. MECHANICAL SPECIFICATION

4.1. Mechanical Dimensions

Figure 2: microSD XL Dimensions (in mm)



SYMBOL	COMMON DIMENSIONS			NOTE
	MIN	NOM	MAX	
A	10.90	11.00	11.10	
A1	9.60	9.70	9.80	
A2	3.85	-	-	BASIC
A3	7.60	7.70	7.80	
A4	-	1.10	-	BASIC
A5	0.75	0.80	0.85	
A6	-	-	8.50	
A7	0.90	-	-	
A8	0.60	0.70	0.80	
A9	0.80	-	-	
A10	1.35	1.40	1.45	
A11	6.50	6.60	6.70	
A12	0.50	0.55	0.60	
A13	0.40	0.45	0.50	
B	14.90	15.00	15.10	
B1	6.30	6.40	6.50	
B2	1.64	1.84	2.04	
B3	1.30	1.50	1.70	
B4	0.42	0.52	0.62	
B5	2.80	2.90	3.00	
B6	5.50	-	-	
B7	0.20	0.30	0.40	
B8	1.00	1.10	1.20	
B9	-	-	9.00	
B10	7.80	7.90	8.00	
B11	1.10	1.20	1.30	
B12	3.60	3.70	3.80	
B13	2.80	2.90	3.00	
B14	8.20	-	-	
B15	-	-	6.20	
C	0.90	1.00	1.10	
C1	0.60	0.70	0.80	
C2	0.20	0.30	0.40	
C3	0.00	-	0.15	
D1	1.00	-	-	
D2	1.00	-	-	
D3	1.00	-	-	
R1	0.20	0.40	0.60	
R2	0.20	0.40	0.60	
R3	0.70	0.80	0.90	
R4	0.70	0.80	0.90	
R5	0.70	0.80	0.90	
R6	0.70	0.80	0.90	
R7	29.50	30.00	30.50	
R10	-	0.20	-	
R11	-	0.20	-	
R17	0.10	0.20	0.30	
R18	0.20	0.40	0.60	
R19	0.05	-	0.20	
R20	0.02	-	0.15	

Notes:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

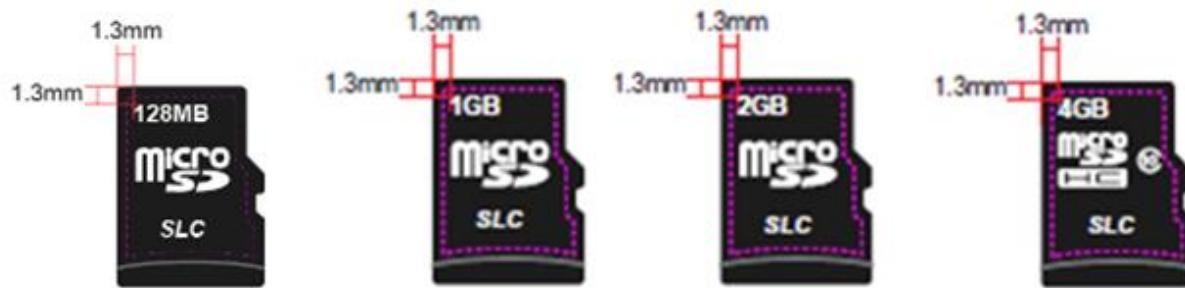
2. DIMENSIONS ARE IN MILLIMETERS.

 COPLANARITY IS ADDITIVE TO C1 MAX THICKNESS.

4.2. Label and Marking

Below are some examples of the standard label for the SMART microSD card.

Figure 3: microSD Label and Marking



5. ELECTRICAL SPECIFICATION

5.1. Electrical Interface

The SMART microSD Memory Cards are fully compliant with the SD specification. The following table describes the I/O signals of the card. Signals whose source is the Host are designated as inputs (I), while signals that the SD Card sources are outputs (O). Bi-directional signals are designated as Input/output (I/O).

Table 6: Pinout Assignments and Pin Types

Pin	Signal Name	Type	Signal Description
1	DAT2	I/O / PP	Data Line [bit2]
2	CD/DAT3	I/O / PP	Card Detect / Data Line [bit3]
3	CMD	PP	Command / Response
4	VCC	S	Supply Voltage
5	CLK	I	Clock
6	GND	S	Supply Voltage Ground
7	DAT0	I/O / PP	Data Line [bit0]
8	DAT1	I/O / PP	Data Line [bit1]

5.2. Absolute Maximum Ratings

Table 7: Absolute Maximum Ratings⁽¹⁾

Parameter	Minimum Value	Maximum Value	Unit
3.3 V Supply Voltage	-0.3	3.6	V
3.3 V Input Voltage	GND - 0.3	Vcc + 0.3	V
Operating Current	128MB, 1GB and 2GB	-	mA
	4GB	-	mA
Operating Temperature – (Commercial)	0	+70	°C
Operating Temperature – (Extended)	-25	+85	°C
Operating Temperature – (Industrial)	-40	+85	°C
Storage Temperature	-40	+85	°C

⁽¹⁾ Stress beyond the Absolute Maximum Rating conditions may result in permanent damage to the device. These are stress ratings only and functional operation should be restricted to those indicated in the operational sections of this specification. Exposure to conditions beyond recommended, up to and including the Absolute Maximum Rating conditions, for extended periods may affect device reliability.

6. DC CHARACTERISTICS

6.1. Bus Operation Conditions for 3.3V Signaling

Table 8: Threshold Level for High Voltage Range

Parameter	Symbol	Min.	Max	Unit	Condition
Supply Voltage	V _{DD}	2.7	3.6	V	
Output High Voltage	V _{OH}	0.75*V _{DD}		V	I _{OH} =-2mA V _{DD} Min
Output Low Voltage	V _{OL}		0.125*V _{DD}	V	I _{OL} =2mA V _{DD} Min
Input High Voltage	V _{IH}	0.625*V _{DD}	V _{DD} +0.3	V	
Input Low Voltage	V _{IL}	V _{SS} -0.3	0.25*V _{DD}	V	
Power Up Time			250	ms	From 0V to V _{DD} min

Table 9: Peak Voltage and Leakage Current

Parameter	Min.	Max	Unit
Peak voltage on all lines	-0.3	V _{DD} +0.3	V
All Inputs			
Input Leakage Current	-10	10	µA
All Outputs			
Output Leakage Current	-10	10	µA

6.2. Bus Operation Conditions for 1.8V Signaling

Table 10: Threshold Level for 1.8 V Signaling

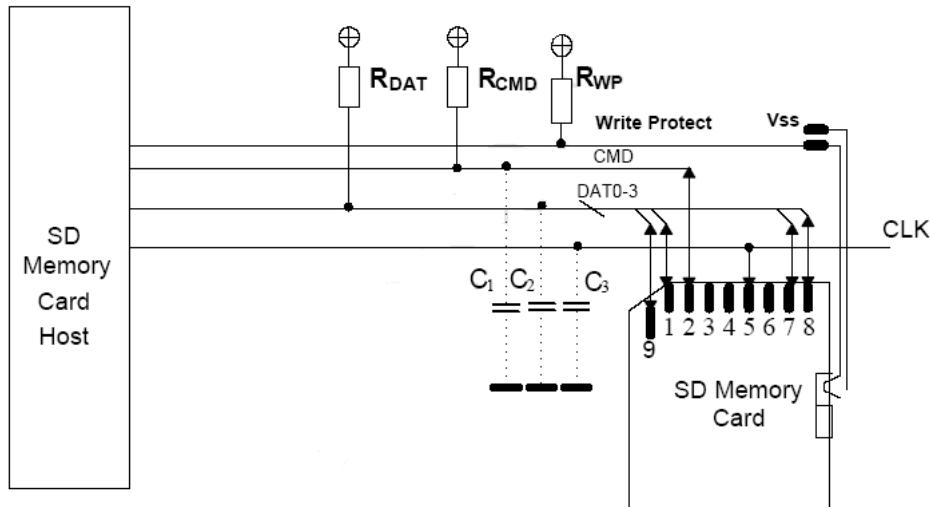
Parameter	Symbol	Min.	Max	Unit	Condition
Supply Voltage	V _{DD}	2.7	3.6	V	
Supply Voltage	V _{DDIO}	1.7	1.95	V	Generated by V _{DD}
Output High Voltage	V _{OH}	1.4		V	I _{OH} =-2mA
Output Low Voltage	V _{OL}		0.45	V	I _{OL} =2mA
Input High Voltage	V _{IH}	1.27	2.00	V	
Input Low Voltage	V _{IL}	V _{SS} -0.3	0.58	V	

Table 11: Input Leakage Current for 1.8V Signaling

Parameter	Min.	Max	Unit	Remarks
Input Leakage Current	-2	2	µA	DAT3 pull-up is disconnected.

6.3. SD Memory Card Hardware Interface

Figure 4: Bus Circuitry Diagram



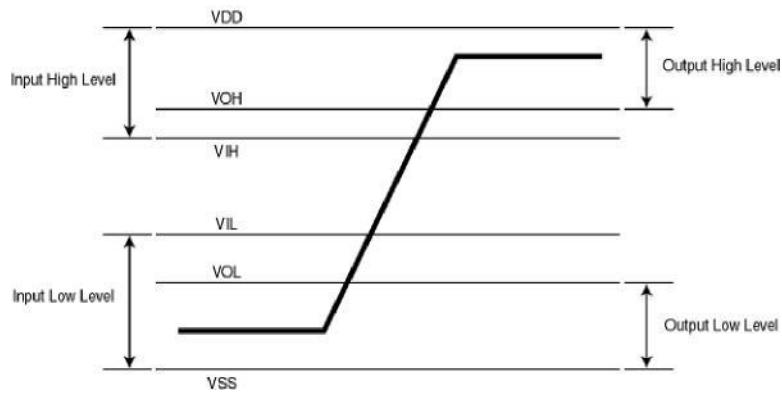
6.4. Bus Signal Line Loading (Recommended)

Table 12: Bus Signal Line Loading (Recommended)

Symbol	Parameter	Min	Max	Units	Remark
R _{CMD}	Pull-up Resistor for CMD Signal	10	100	kΩ	to prevent bus floating
R _{DAT}	Pull-up Resistor for DAT Signals	10	100	kΩ	to prevent bus floating
C _L	Total bus capacitance for each signal line		40	pF	1 card C _{HOST} +C _{BUS} shall not exceed 30 pF
C _{CARD}	Card Capacitance for each signal pin		10	pF	
-	Maximum signal line inductance		16	nH	
R _{DAT3}	Pull-up resistance inside card	10	90	kΩ	May be used for card detection
C _c	Capacity Connected to Power Line		5	μF	To prevent inrush current

7. AC CHARACTERISTICS

Figure 5: Bus Signal Level



7.1. Interface Timing (Default Speed Mode)

Figure 6: Card Input Timing (Default Speed Mode)

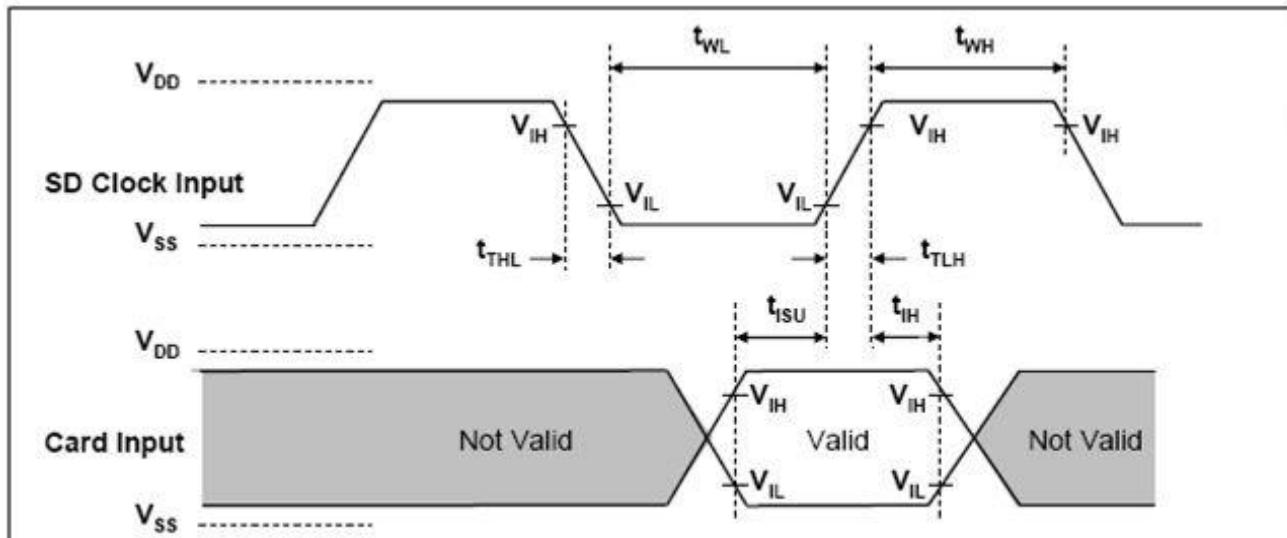


Figure 7: Card Output Timing (Default Mode)

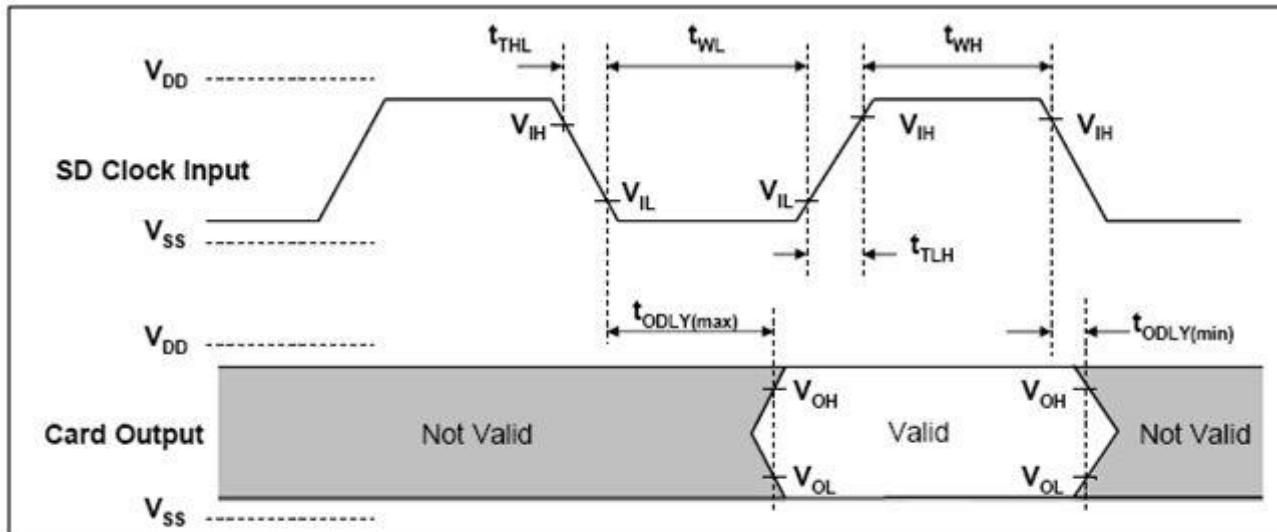


Table 13: Bus Timing (Default Speed Mode)

Symbol	Parameter	Min	Max	Unit	Remark ⁽¹⁾
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL})					
f _{PP}	Clock frequency data transfer mode	0	25	MHz	C _{card} ≤ 10 pF
f _{OD}	Clock	0 ⁽²⁾ /100	400	kHz	
t _{WL}	Clock low time	10		ns	C _{card} ≤ 10 pF
t _{WH}	Clock high time	10		ns	C _{card} ≤ 10 pF
t _{TLH}	Clock rise time		10	ns	C _{card} ≤ 10 pF
t _{THL}	Clock fall time		10	ns	C _{card} ≤ 10 pF
Inputs CMD, DAT (referenced to CLK)					
t _{ISU}	Input setup time	5		ns	C _{card} ≤ 10 pF
t _{IH}	Input hold time	5		ns	C _{card} ≤ 10 pF
Outputs CMD, DAT (referenced to CLK)					
t _{ODLY}	Output delay time during Data Transfer Mode	0	14	ns	C _L ≤ 40 pF
t _{ODLY}	Output delay time during Data Identification mode	0	50	ns	C _L ≤ 40 pF

⁽¹⁾ Values are for 1 card.

⁽²⁾ 0Hz means to stop the clock. The given minimum frequency range is for cases where continuous clock is required.

7.2. Interface Timing (High Speed Mode)

Figure 8: Input Timing (High Speed Mode)

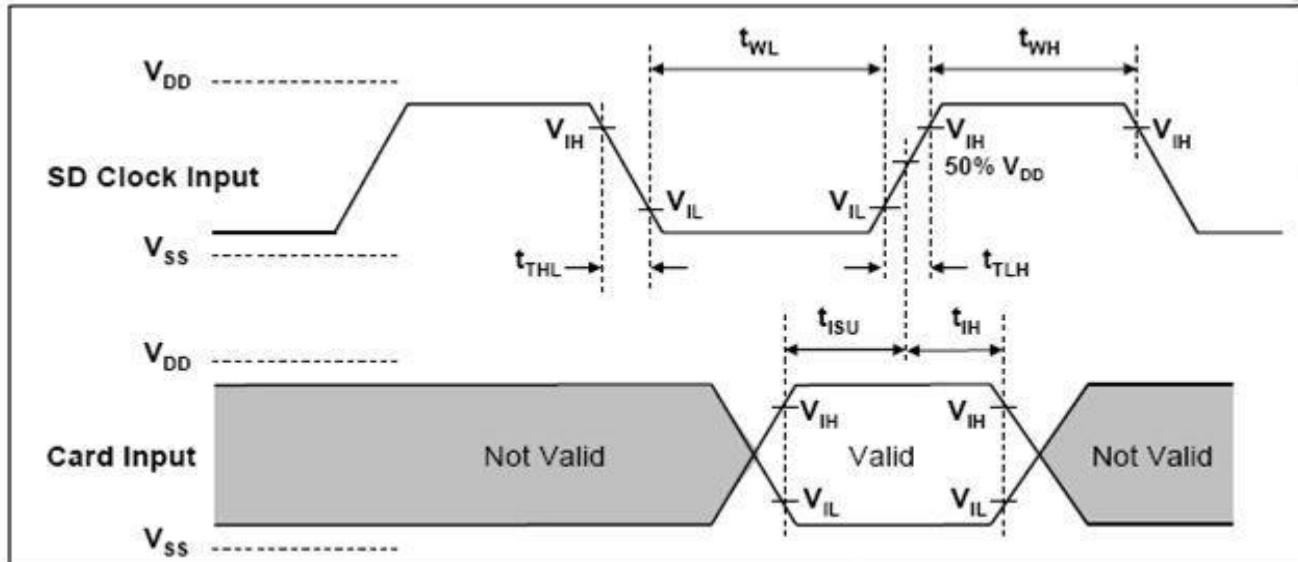


Figure 9: Output Timing (High Speed Mode)

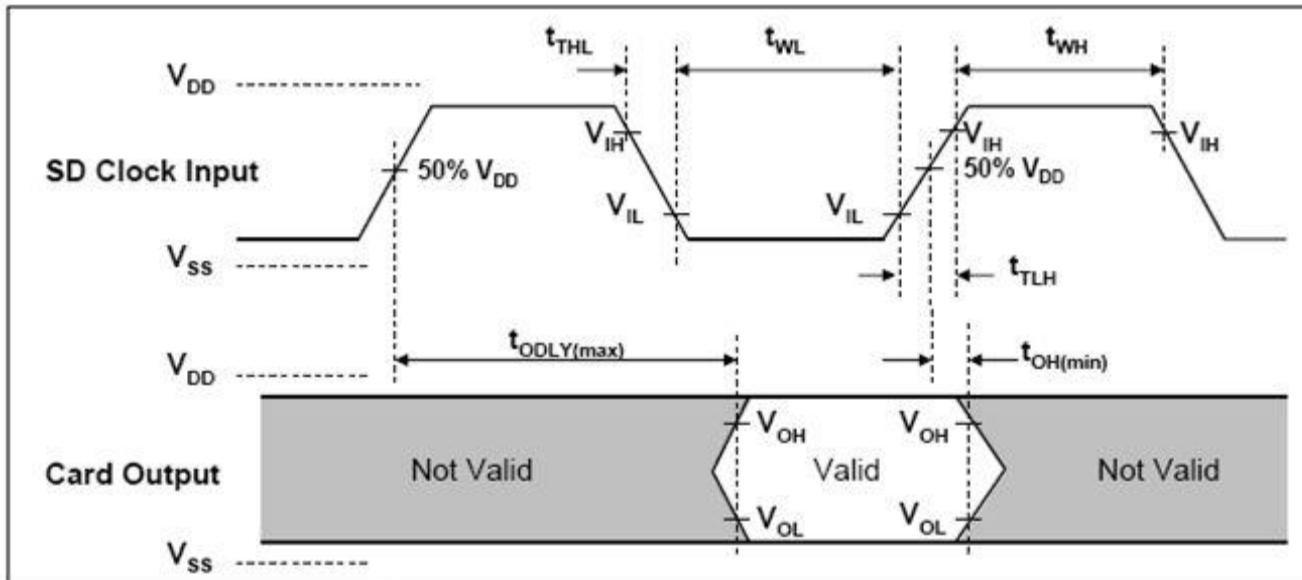
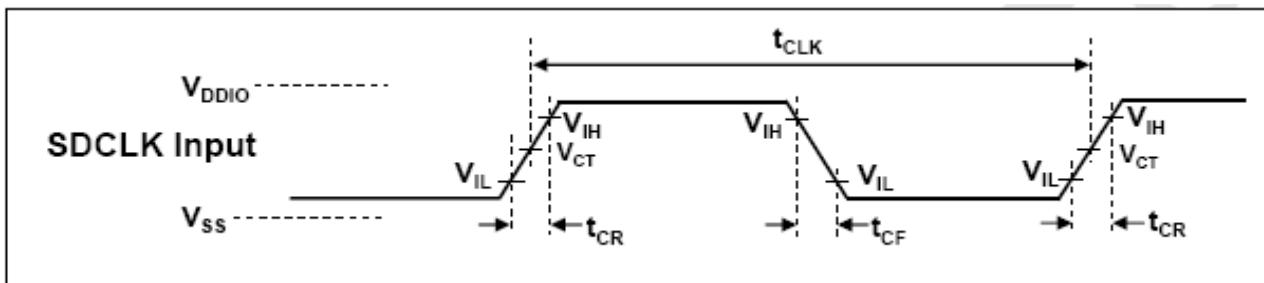


Table 14: Bus Timing (High Speed)

Symbol	Parameter	Min	Max	Unit	Remark ⁽¹⁾
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL}))					
f_{PP}	Clock frequency data transfer mode	0	50	MHz	$C_{card} \leq 10 \text{ pF}$
t_{WL}	Clock low time	7	-	ns	$C_{card} \leq 10 \text{ pF}$
t_{WH}	Clock high time	7	-	ns	$C_{card} \leq 10 \text{ pF}$
t_{TLH}	Clock rise time	-	3	ns	$C_{card} \leq 10 \text{ pF}$
t_{THL}	Clock fall time	-	3	ns	$C_{card} \leq 10 \text{ pF}$
Inputs CMD, DAT (referenced to CLK)					
t_{IS}	Input setup time	6	-	n	$C_{card} \leq 10 \text{ pF}$
t_i	Input hold time	2	-	n	$C_{card} \leq 10 \text{ pF}$
Outputs CMD, DAT (referenced to CLK)					
t_{ODLY}	Output delay time during Data Transfer Mode	-	14	ns	$C_L \leq 40 \text{ pF}$
t_{OH}	Output Hold Time	2.5	-	ns	$C_L \leq 40 \text{ pF}$
C_L	Total System Capacitance of each line	-	40	pF	$C_L \leq 15 \text{ pF}$

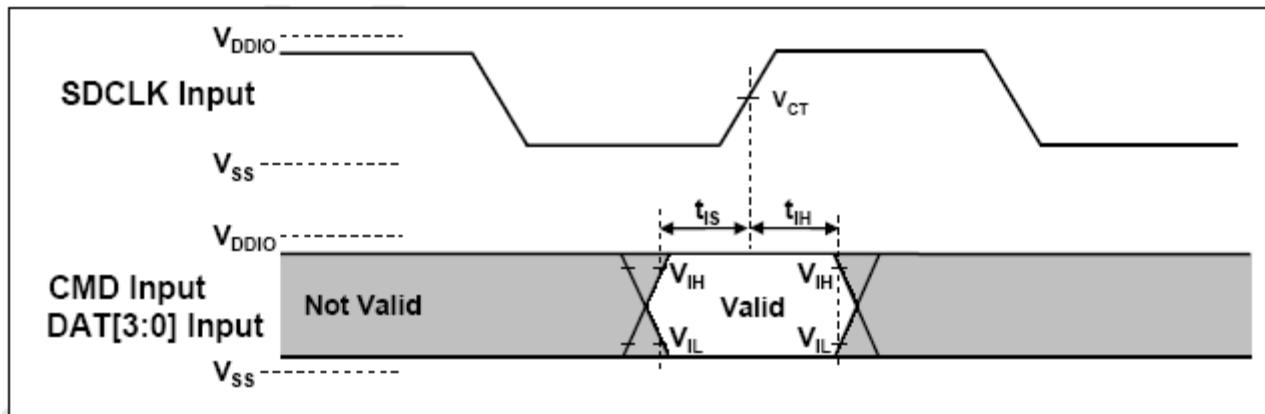
⁽¹⁾ In order to satisfy server timing, host shall drive only one card.

7.3. Interface Timing (SDR12, SDR25 and SDR50 Modes)

Figure 10: Input Clock Signal Timing


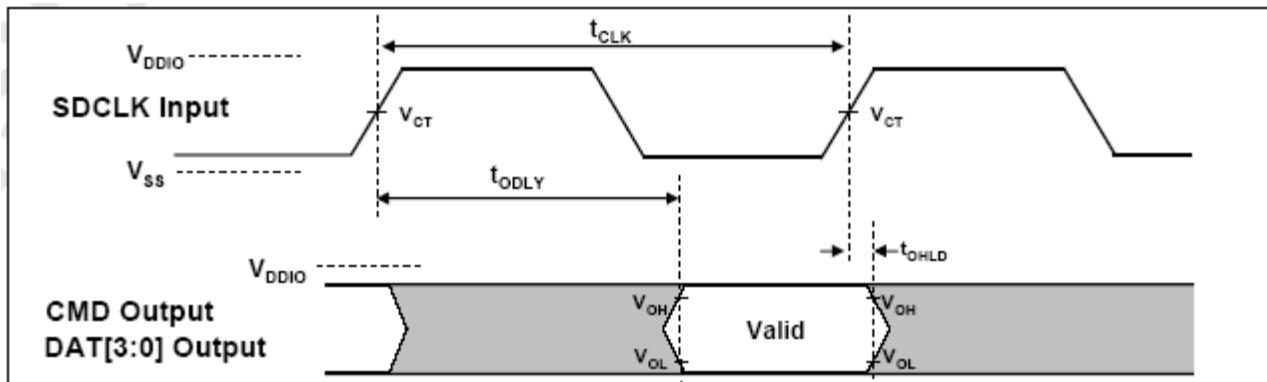
Symbol	Min	Max	Unit	Remark
t_{CLK}	4.80	-	ns	208MHz (Max), Between rising edge, $V_{CT} = 0.975V$
t_{CR}, t_{CF}	-	$0.2 * t_{CLK}$	ns	$t_{CR}, t_{CF} < 2.00\text{ns}$ (max) at 100 MHz, $C_{CARD} = 10\text{pF}$
Clock Duty	30	70	%	

Figure 11: Card Input Timing (SDR50)



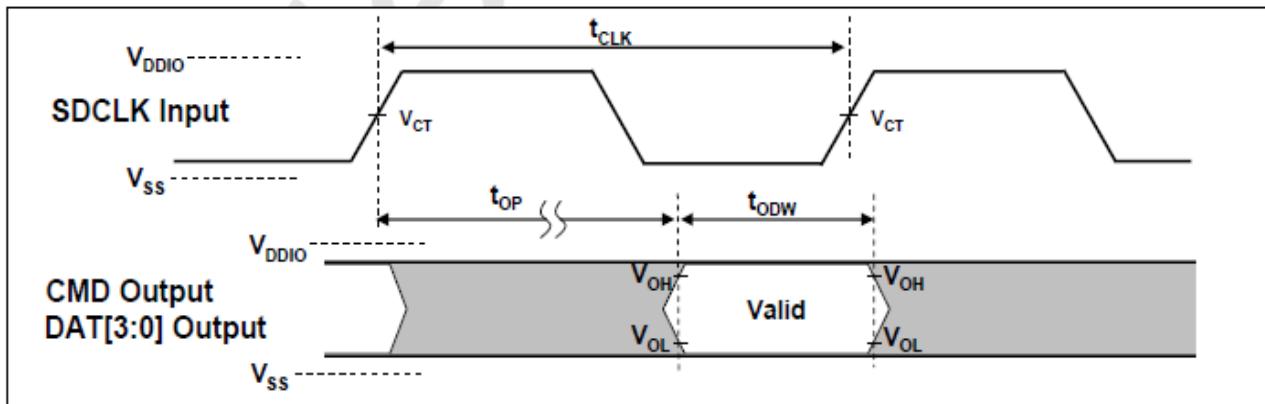
Symbol	Min	Max	Unit	SDR104 mode
t_{IS}	1.40	-	ns	$C_{CARD} = 10\text{pF}, V_{CT} = 0.975\text{V}$
t_{IH}	0.80	-	ns	$C_{CARD} = 5\text{pF}, V_{CT} = 0.975\text{V}$
Symbol	Min	Max	Unit	SDR50 mode
t_{IS}	3.00	-	ns	$C_{CARD} = 10\text{pF}, V_{CT} = 0.975\text{V}$
t_{IH}	0.80	-	ns	$C_{CARD} = 5\text{pF}, V_{CT} = 0.975\text{V}$

Figure 12: Output Timing - Fixed Data Window (SDR12, SDR25, SDR50)



Symbol	Min	Max	Unit	Remark
t_{ODLY}	-	7.5	ns	$t_{CLK} \geq 10.0\text{ns}$, $C_L = 30\text{pF}$, using driver Type B, for SDR50
t_{ODLY}	-	14	ns	$t_{CLK} \geq 20.0\text{ns}$, $C_L = 40\text{pF}$, using driver Type B, for SDR25 and SDR12
t_{OH}	1.5	-	ns	Hold time at the t_{ODLY} (min.), $C_L = 15\text{pF}$

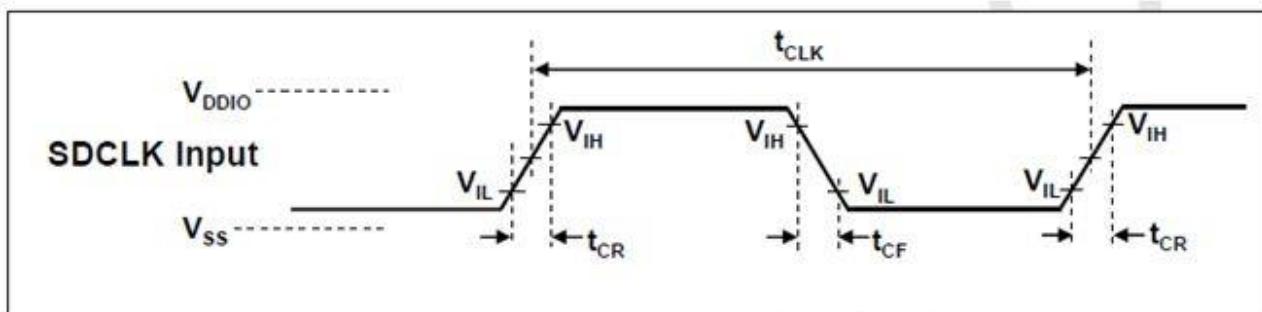
Figure 13: Output Timing - Variable Window (SDR104)



Symbol	Min	Max	Unit	Remark
t_{OP}	0	2	UI	Card Output Phase
Δt_{OP}	-350	+1550	ps	Delay variation due to temperature change after tuning
t_{ODW}	0.60	-	UI	$t_{ODW} = 2.88\text{ns}$ at 208MHz

7.4. Interface Timing (DDR50 Mode)

Figure 14: Interface Timing (DDR50 Mode)



Symbol	Min	Max	Unit	Remark
t_{CLK}	20	-	UI	50MHz (Max) Between rising edge
t_{CR}	-	$0.2 * t_{CLK}$	ns	$t_{CR}, t_{CF} < 4.00\text{ns}$ (max) at 50MHz, CCARD = 10pF
Clock Duty	45	55	%	

Figure 15: DAT Inputs/Outputs Referenced to CLK in DDR50 Mode

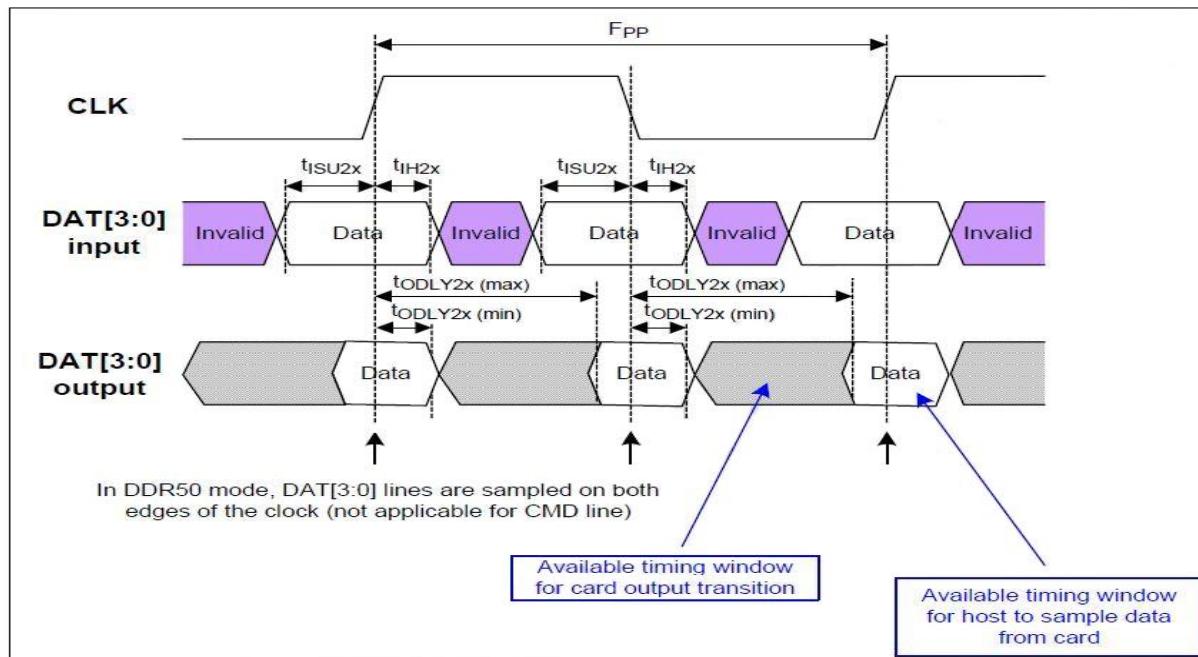


Table 15: Bus Timings – Parameters Values (DDR50 Mode)

Parameter	Symbol	Min	Max	Unit	Remark
Input CMD (referenced to CLK rising edge)					
Input set-up time	t _{ISU}	6	-	ns	C _{card} ≤ 10 pF (1 card)
Input hold time	t _{IH}	0.8	-	ns	C _{card} ≤ 10 pF (1 card)
Output CMD (referenced to CLK rising edge)					
Output Delay time during Data Transfer Mode	t _{ODLY}	-	13.7	ns	C _L ≤30 pF (1 card)
Output Hold time	t _{OH}	1.5	-	ns	C _L ≥15 pF (1 card)
Inputs DAT (referenced to CLK rising and falling edges)					
Input set-up time	t _{ISU2x}	3	-	ns	C _{card} ≤ 10 pF (1 card)
Input hold time	t _{IH2x}	0.8	-	ns	C _{card} ≤ 10 pF (1 card)
Outputs DAT (referenced to CLK rising and falling edges)					
Output Delay time during Data Transfer Mode	t _{ODLY2x}	-	7.0	ns	C _L ≤25 pF (1 card)
Output Hold time	t _{OH2x}	1.5	-	ns	C _L ≥15 pF (1 card)

8. REGISTERS

The registers are used in the SMART SD cards are shown in the table below. These registers are described in the sections that follow.

Table 16: Supported SD Registers

Name	Width	Description
CID	128	Card Identification
RCA	16	Relative Card Address
CSD	128	Card Specific Data
SCR	64	SD Configuration Register
OCR	32	Operation Condition Register
SSR	512	SD Status Register

8.1. Card Identification Register (CID)

The Card Identification (CID) register is 128 bits wide. It contains the information used during the card identification phase. Every individual flash card will have a unique identification number. The fields for the CID register are presented in the following table.

Table 17: Card Identification Register (CID) Fields

Bits	Width	Name	Field	Value
[127:120]	8	Manufacturer ID	MID	27h
[119:104]	16	OEM/Application ID	OID	5048h
[103:64]	40	Product Name	PNM	128MB SD128
				1GB SD01G
				2GB SD02G
				4GB SD04G
[63:56]	8	Product Revision	PRV	3.0 (30h) ⁽¹⁾
[55:24]	32	Product Serial Number	PSN	-- ⁽²⁾
[23:20]	4	Reserved	--	--
[19:8]	12	Manufacturing Date	MDT	-- ⁽²⁾
[7:1]	7	CRC7 Checksum	CRC	-- ⁽²⁾
[0]	1	Not used, Always 1	-	1b

⁽¹⁾ Supports SD Spec 3.0

⁽²⁾ The value is defined by the default setting.

8.2. Relative Card Address (RCA)

The Relative Card Address (RCA) register is 16 bits wide. It contains the card address assigned by the host during the card identification. This address is used for the addressed host-card communication after the identification procedure. The default value of the RCA register is 0x0000.

8.3. Card Specific Data (CSD)

The Card Specific Data (CSD) register is 128 bits wide. It provides information on how to access the card contents. The fields for the CSD register are presented in the following table.

Table 18: CSD Version 1.0 - 1GB and 2GB Register Table

Bits	Width	Name	Field	Value
[127:126]	2	CSD structure	CSD_STRUCTURE	00b
[125:120]	6	Reserved	---	---
[119:112]	8	Data read access time 1	TAAC	5Eh
[111:104]	8	Data read access time 2	NSAC	00h
[103:96]	8	Max. bus clock frequency	TRAN_SPEED ⁽³⁾	5Ah
[95:84]	12	Card command classes	CCC ⁽¹⁾	5B5h
[83:80]	4	Max read block data length	READ_BL_LEN ⁽⁴⁾	128MB 1GB 2GB Ah
[79]	1	Partial block read allowed	READ_BL_PARTIAL	1b
[78]	1	Write block misalignment	WRITE_BLK_MISALIGN	0b
[77]	1	Read block misalignment	READ_BLK_MISALIGN	1b
[76]	1	DSR implemented	DSR_IMP	0b
[75:74]	2	Reserved	---	---
[73:62]	12	Device size	C_SIZE ⁽²⁾	128MB 1GB 2GB 1110 1010 0111b 1110 1101 1011b 1110 1100 0011b
[61:59]	3	Max read current@ VDD min	VDD_R_CURR_MIN	111b
[58:56]	3	Max read current@ VDD max	VDD_R_CURR_MAX	111b
[55:53]	3	Max write current@ VDD min	VDD_W_CURR_MIN	111b
[52:50]	3	Max write current@ VDD max	VDD_W_CURR_MAX	111b
[49:47]	3	Device size multiplier	C_SIZE_MULT	128MB 1GB 2GB 100b 111b 111b
[46]	1	Erase single block enable	ERASE_BLK_EN	1b
[45:39]	7	Erase sector size	SECTOR_SIZE	111 1111b
[38:32]	7	Write protect group size	WP_GRP_SIZE	0000000b
[31]	1	Write protect group enable	WP_GRP_ENABLE	0b
[30:29]	2	Reserved	---	---
[28:26]	3	Write speed factor	R2W_FACTOR	010b
[25:22]	4	Max write data block length	WRITE_BL_LEN ⁽⁴⁾	128MB 1GB 2GB 9h 9h Ah
[21]	1	Partial block write allowed	WRITE_BL_PARTIAL	0b
[20:16]	5	Reserved	---	---
[15]	1	File format group	FILE_FORMAT_GRP	0b
[14]	1	Copy Flag	COPY	0b
[13]	1	Permanent write protection	PERM_WRITE_PROTECT	0b
[12]	1	Temporary write protection	TMP_WRITE_PROTECT	0b
[11:10]	2	File Format	FILE_FORMAT	00b
[9:8]	2	Reserved	---	---
[7:1]	7	CRC	CRC ⁽²⁾	--
[0]	1	Not used, always '1'	---	1

(1) Support command class: 0, 2, 4, 5, 7, 8 and 10. (Including Basic, Block Read/Write, Erase, Lock Card, Application specific and switch. Not supported command class: 1, 3, 6 and 9(Including Write-Protection, I/O mode)

(2) This field depends upon the flash used with the controller.

(3) Value depends on the Card Type and mode.

(4) READ_BL_LEN / WRITE_BL_LEN: 9h = 512 Byte; Ah = 1024 Byte.

Table 19: CSD Version 2.0 - 4GB Register Table

Bits	Width	Name	Field	Value
[127:126]	2	CSD Structure	CSD_STRUCTURE	01b
[125:120]	6	Reserved	---	00 0000b
[119:112]	8	Data Read Access Time 1	TAAC	0Eh
[111:104]	8	Data Read Access Time 2	NSAC	00h
[103:96]	8	Max. Bus Clock Frequency	TRAN_SPEED ⁽⁴⁾	32h
[95:84]	12	Card Command Classes	CCC ⁽¹⁾	5B5h
[83:80]	4	Max Read Block Data Length	READ_BL_LEN ⁽³⁾	9h
[79]	1	Partial Block Read Allowed	READ_BL_PARTIAL	0b
[78]	1	Write Block Misalignment	WRITE_BLK_MISALIGN	0b
[77]	1	Read Block Misalignment	READ_BLK_MISALIGN	0b
[76]	1	DSR implemented	DSR_IMP	0b
[75:70]	6	Reserved	---	00 0000b
[69:48]	22	Device Size	C_SIZE ⁽²⁾	01 1101 1010 1011b
[47]	1	Reserved	---	0b
[46]	1	Erase Single Block Enable	ERASE_BLK_EN	1b
[45:39]	7	Erase Sector Size	SECTOR_SIZE	111 1111b
[38:32]	7	Write Protect Group Size	WP_GRP_SIZE	000 0000b
[31]	1	Write Protect Group Enable	WP_GRP_ENABLE	0b
[30:29]	2	Reserved	---	00b
[28:26]	3	Write Speed Factor	R2W_FACTOR	010b
[25:22]	4	Max Write Data Block Length	WRITE_BL_LEN ⁽³⁾	9h
[21]	1	Partial Block Write Allowed	WRITE_BL_PARTIAL	0b
[20:16]	5	Reserved	---	0 0000b
[15]	1	File Format Group	FILE_FORMAT_GRP	0b
[14]	1	Copy Flag	COPY	0b
[13]	1	Permanent Write Protection	PERM_WRITE_PROTECT	0b
[12]	1	Temporary Write Protection	TMP_WRITE_PROTECT	0b
[11:10]	2	File Format	FILE_FORMAT	00b
[9:8]	2	Reserved	---	00b
[7:1]	7	CRC	CRC	--
[0]	1	Not used, Always '1'	---	1

(1) Support command class: 0, 2, 4, 5, 7, 8 and 10.(Including Basic, Block Read/Write, Erase, Lock Card, Application specific and switch. Not supported command class: 1, 3, 6 and 9(Including Write-Protection, I/O mode)

(2) This field depends upon the flash used with the controller.

(3) This field is fixed to 9h, which indicates READ_BL_LEN / WRITE_BL_LEN = 512 Byte.

(4) Value depends on the Card Type and mode.

8.4. SD Configuration Register (SCR)

The SD Configuration Register (SCR) is 64 bits wide. It is another configuration register. SCR provides information about the SD card's special features that were configured into the given card. The fields for the SCR register are presented in the following table.

Table 20: SD Configuration Register (SCR) Fields

Bits	Width	Name	Field	Value (Binary)
[63:60]	4	SCR Structure	SCR_STRUCTURE	0000
[59:56]	4	SD Card Spec. Version	SD_SPEC	0010
[55]	1	Data Status After Erase	DATA_STAT_AFTER_ERASE	0
[54:52]	3	CPRM Security Support	SD_SECURITY	128MB/ 1GB/2GB
				4GB
				011
[51:48]	4	DAT Bus Width Support	SD_BUS_WIDTHS	0101
[47]	1	Spec. Version 3.00 or Higher	SD_SPEC3	1
[46:43]	4	Extended Security Support	EX_SECURITY	0000
[42:34]	9	Reserved	-	-
[33:32]	2	Command Support bits	CMD_SUPPORT	128MB/ 1GB/2GB
				4GB
[31:0]	32	Reserved for manufacturer usage	-	-

8.5. Operation Condition Register (OCR)

The Operation Condition Register (OCR) register is 32 bits wide. The fields for the OCR register are presented in the following table.

Table 21: Operation Condition Register (OCR) Fields

Bits	Width	VDD Voltage Window	Value (Binary)
[0:6]	7	Reserved	0000
[7]	1	Reserved for Low Voltage Range	0
[8:14]	7	Reserved	000 0000
[15]	1	2.7-2.8	1
[16]	1	2.8-2.9	1
[17]	1	2.9-3.0	1
[18]	1	3.0-3.1	1
[19]	1	3.1-3.2	1
[20]	1	3.2-3.3	1
[21]	1	3.3-3.4	1
[22]	1	3.4-3.5	1
[23]	1	3.5-3.6	1
[24]	1	Switching to 1.8V Accepted (S18A)	-- (1)
[25:29]	5	Reserved	00 0000
[30]	1	Card Capacity Status (CCS)	--(2)
[31]	1	Card power up status bit	1 ⁽³⁾

(1) Only UHS-I card supports this bit.

(2) This bit is valid only when the card power up status bit is set.

(3) This bit is set to LOW if the card has not finished the power up routine.

8.6. SD Status Register

The SD Status Register (SSR) is 512 bits wide and provides information about the SD card's proprietary and may be used for application-specific usage. The fields for the SSR register are presented in the following table.

Table 22: SD Status Register (SSR) Fields

Bits	Width	Field	Value	
[511:510]	2	DAT_BUS_WIDTH	10b	
[509]	1	SECURED_MODE	0b	
[508:502]	7	Reserved	--	
[501:496]	6	Reserved	--	
[495:480]	16	SD_CARD_TYPE	0000h	
[479:448]	32	SIZE_OF_PROTECTED_AREA	128MB	00000028h
			1GB	00000028h
			2GB	00000028h
			4GB	02000000h
[447:440]	8	SPEED_CLASS	128MB	01h (Class 2)
			1GB	03h (Class 6)
			2GB	03h (Class 6)
			4GB	04h (Class 10)
[439:432]	8	PERFORMANCE_MOVE	128MB	01h (1 MB/sec)
			1GB	03h (3 MB/sec)
			2GB	03h (3 MB/sec)
			4GB	00h (0 MB/sec)
[431:428]	4	AU_SIZE	9h (4MB)	
[427:424]	4	Reserved	--	
[423:408]	16	ERASE_SIZE	0200h (512 AU)	
[407:402]	6	ERASE_TIMEOUT	10 1010b (42 sec)	
[401:400]	2	ERASE_OFFSET	11b (3 sec)	
[399:396]	4	UHS_SPEED_GRADE ⁽²⁾	128MB/ 1GB/2GB	Not applicable
			4GB	1h (10MB/sec and above)
[395:392]	4	UHS_AU_SIZE	128MB/ 1GB/2GB	Not applicable
			4GB	Fh (64 MB)
[391:312]	80	Reserved	--	
[311:0]	312	Reserved	Reserved for manufacturer	

9. PART NUMBERS

9.1. Part Numbering Information

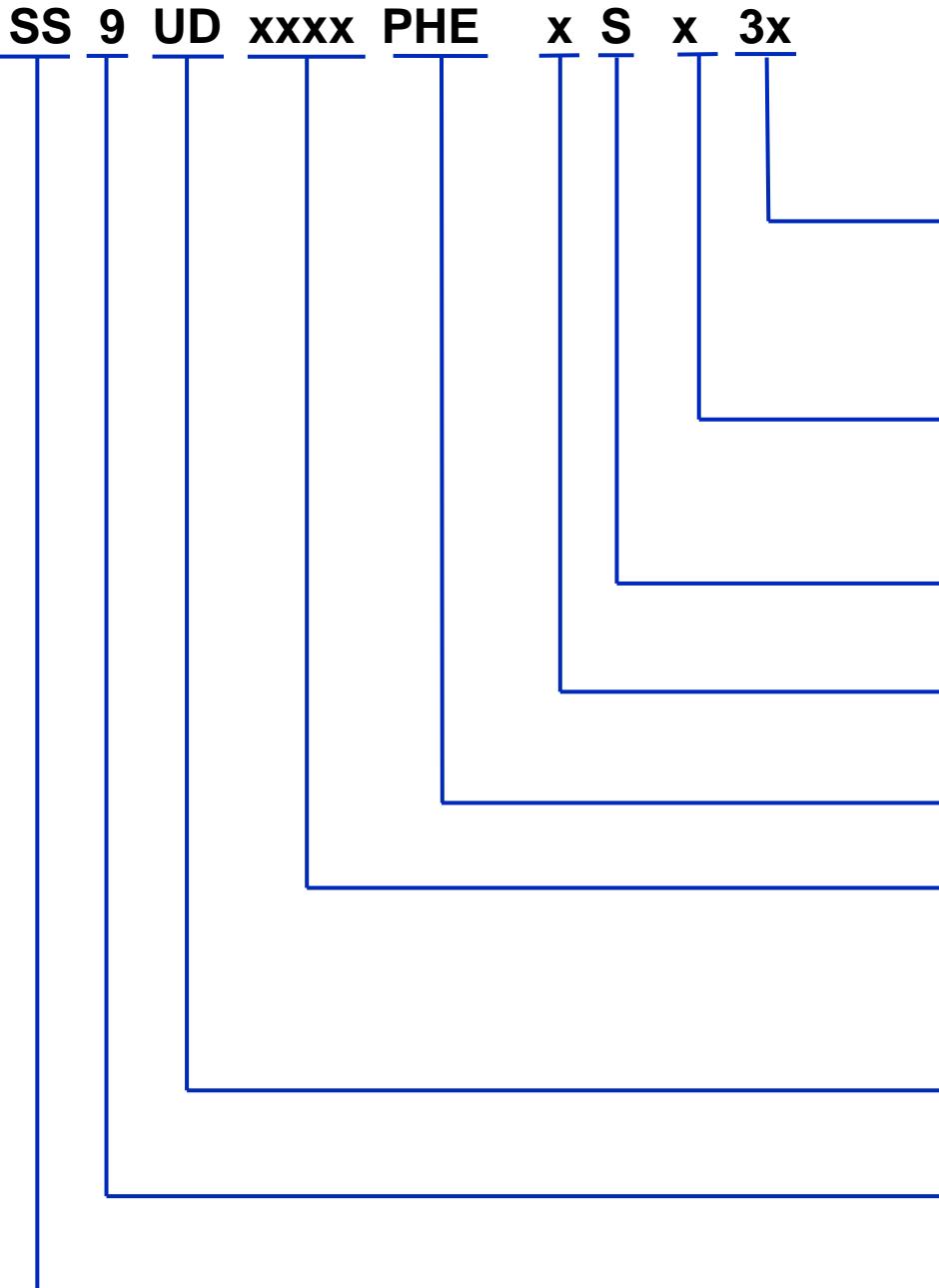
Table 23: Part Numbering Information

SMART Part Number	Capacity	User Formatted Capacity (Bytes)	Unformatted Capacity (C-Size correlated) (Bytes)
SS9UD128MPHE6SC31	128MB	122,847,232	122,945,536
SS9UD001GPHE8Sx31	1 GB	996,868,096	997,195,776
SS9UD002GPHE8Sx31	2 GB	1,981,480,960	1,981,808,640
SS9UD004GPHE8Sx31	4 GB	3,974,103,040	3,982,491,648
SS9UD001GPHE8Sx32	1 GB	996,868,096	997,195,776
SS9UD002GPHE8Sx32	2 GB	1,981,480,960	1,981,808,640
SS9UD004GPHE8Sx32	4 GB	3,974,103,040	3,982,491,648

x = E: Extended Temperature Range (-25°C to +85°C)

x = I: Industrial Temperature Range (-40°C to +85°C)

9.2. Part Number Decoder



Release Version

Flash Rev / Initial release
 32: Release New Firmware
 31: Toshiba 24nm
 01: Initial release

Temperature Rating

C: Commercial 0°C to 70°C
 E: Extended -25°C to 85°C
 I: Industrial -40°C to 85°C

Flash Technology

S: SLC

Flash Device Density

6: 1Gbit
 8: 4Gbit

Controller

PHE: PS8210DF

Capacity

128M: 128MB
 001G: 1GB
 002G: 2GB
 004G: 4GB

Product Type

UD: Micro-SD 11x15x1mm

Memory Cards

SMART Modular
 SS: Specialty, ROHS

10. DECLARATION OF CONFORMITY

Responsible Party Name: SMART Modular Technologies, Inc.
Address: 39870 Eureka Drive
Newark, CA 94560-4809, USA
Phone: +1-510-623-1231

Hereby declares that the products:

SS9UDxxxxPHExSx3x

to which this declaration relates are in conformity with the following Directives and other normative documents:

RoHS Directive 2011/65/EU

Restriction of the use of certain hazardous substances in electrical and electronic equipment

- **EN 50581:2012**
Technical documentation for the assessment of electrical and electronic products with respect to the restriction of hazardous substances

Name: Jeffrey Milano
Title: Director, Worldwide Quality
Date: March 30, 2018 11:48 AM

Representative in the European Union (for regulatory topics only):

Mr. Graham Kyle
SMART Modular Technologies (Europe) Ltd.
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