PRETEC® Datasheet

iSD / iSDHC 100 & 300
Industrial SD Card

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PRETEC/C-ONE TECHNOLOGY CORP.

CONTENT

1. Introduction

1.1 General Description

Pretec iSD / iSDHC 100 and iSDHC 300 are high speed features innovative SLC Nand flash memory system, the capacity are 256MB to 32GB. It is fully compatible with the SD card transmission specification standard which highlights synchronous serial interface optimized for fast and reliable data transmission. It features very low operation power consumption, low standby power consumption and automatically power saving sleep control and operate with wide voltage range from 2.7V to 3.6V.

Two data transmission modes: SD compatible SPI mode that allow more flexible host device access control. Cyclic redundancy check (CRC) code at the end of each data transmission provides real time error detection. This is the best solution for PDA, PND, DSC, Digital Camcorder and Industrial Equipment as a storage device.

1.2 Features

System standard compatibility

— Support SD and SDHC compatible flash Memory Card interface.
— Fully compatible with SD Standard: iSD / iSDHC 100 (SD2.0), iSDHC 300 (SD3.0)
— Configurable SD-1, SD-4 or SPI Flash Memory Card interface.
— Automatic wake up from power-down on host reset or command write.
— Automatic sleep down after 3 seconds card stand-by.
— Sector data transfers without microprocessor intervention.

Flash Memory Control:

— Flash Sequencer Logic to support all the control signals to execute read/write/erase operation automatically.
— Flash Write Protect control support.
— High speed Flash Read/Write performance.
— Global Wear Leveling.
— Configurable 24~72-bit/1KB BCH hardware ECC.

Low power

— 2.7V to 3.6V power supply.
— Built-in card reset with supply voltage < 2.7V

SMART Function support

2. Product part number

The C-ONE iSD/iSDHC provides robust storage medium and consists of a wide range of capacities as described below**:**

iSD / iSDHC 100 series:

Capacity	Order Part Number
256MB	SDI100256MP-HA
512MB	SDI100512MP-HA
1GB	SDI100001GP-HA
2GB	SDI100002GP-HA
4GB	SDI100004GP-HA

iSDHC 300 series:

Capacity	Order Part Number
8GB	SDI300008GP-HA
16GB	SDI300016GP-HA
32GB	SDI3000132GP-HA

3. Physical description

1.Weight and Measures	iSD/ iSDHC	Dimensions:
		32mm(L) x 24mm(W) x 2.1mm(H)
		Weight: 2.0g max
2.Voltage Range	Power modes	Basic communication (CMD0, CMD8, CMD15, CMD55, ACMD41): 2.7 ~ 3.6 V1
		SDLV Memory Card (low voltage) - Operating voltage range: 1.6 ~ 3.6 V2
3.Typical Power Consumptions:	Voltage 3.3V	Read Mode: 25mA max
		Write Mode: 25mA max
		Standby: 130µA max

4.Performance:	Data Transfer Rates	Series	Capacity	Read/Write Speed
		iSD 100	256MB~512MB	Up to 18MB/ Up to 10MB
		iSD 100	1GB~4GB	Up to 23MB/ Up to 16MB
		iSD 300	8GB	Up to 30MB/ Up to 20MB
		iSD 300	16GB~32GB	Up to 60MB/ Up to 55MB

5.Environment Conditions:	MTBF	3,000,000 hours
	Operating Temperature	-40°C to 85°C
	Storage Temperature	-50°C to 95°C
	Shock	50G duration 0.5ms half sine wave
	Vibration	5Gpeak 7~2000Hz with (15mins/Axis) 3axis
	Humidity	5% to 95%

4. Block Diagram
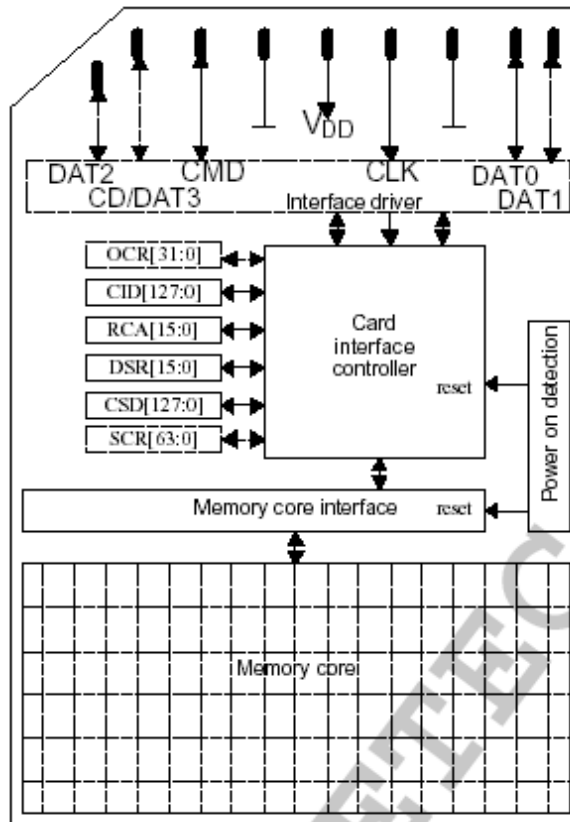
5. Interface

These C-ONE SDHC interface can operate in two different modes:

— SD compatible mode: SD 1-bit mode, SD 4-bit mode

— SPI mode

Both modes use the same pins and the default mode is the SD 1-bit mode. The SPI mode is selected by activating (=0) the CS signal (Pin 1) and sending the CMD1.

SD Compatible Mode

In the SD compatible mode, all data is transferred over a minimal number of lines:

— **CLK:** Host to card clock signal

— **CMD:** Bidirectional Command/Response signal

— **DAT0-3:** 4 Bidirectional data signals

— **VDD, VSS1, VSS2:** Power and ground signals
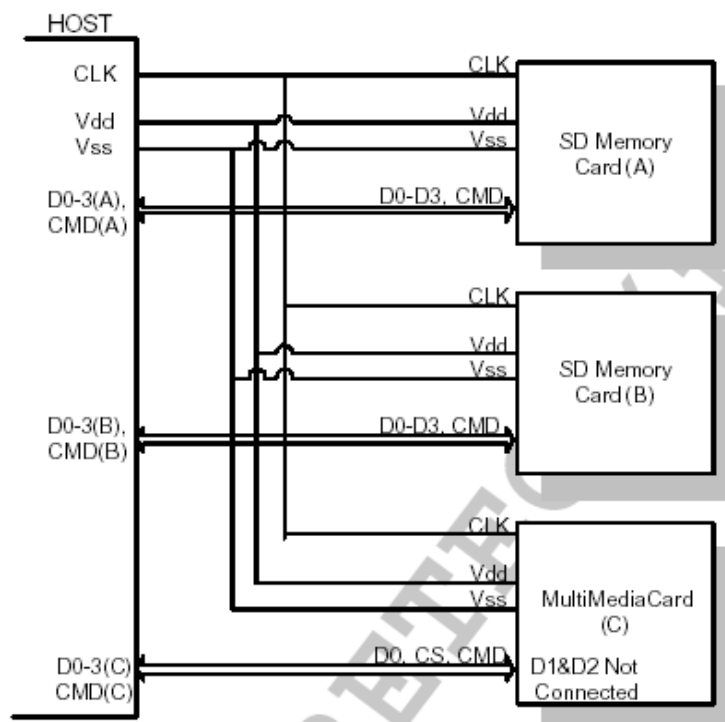
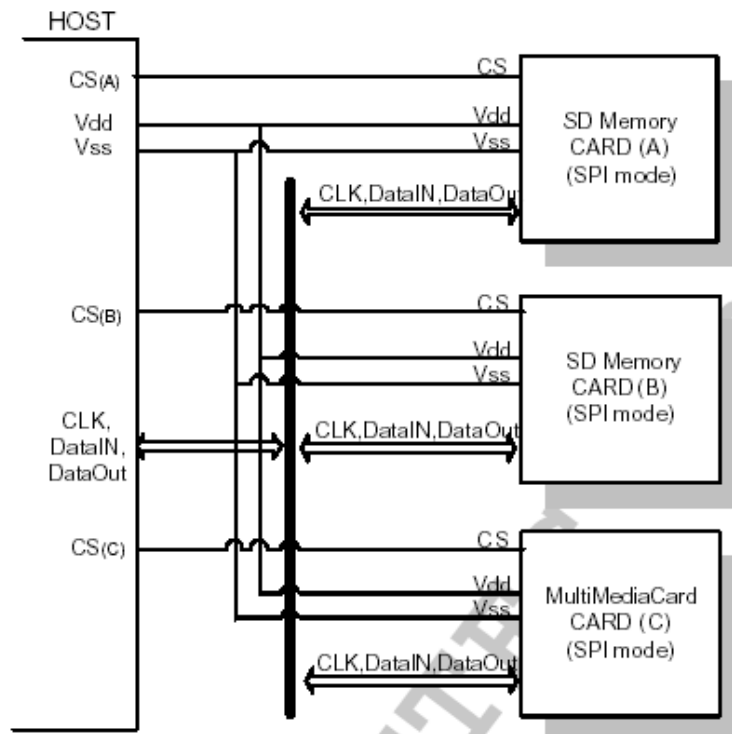**SD Memory Card system bus Topology**

The SD bus has a signal master (application host), multiple slaves (cards), and synchronous star topology. Clock, power and ground signals are common to all cards. Command (CMD) and data (DAT0-3) signals are dedicated to each SD or SDHC providing continuous point-to-point connection. During initialization process commands are sent to each card individually, allowing the application to detect the cards and assign logical addresses to the physical slots. Data is always sent (received) to (from) each card individually. SD bus allows dynamic configuration fit the number of data lines. After power up, by default, the SD card will use only DAT0 for data transfer. After initialization the host may change the bus width to enhance the data transmission (number of active data lines.

6. SPI Mode

The SPI compatible communication mode, a subset of SD memory card protocol, is designed to communicate with a SPI channel, commonly found in various microcontrollers in the market. The interface is selected during the first reset command after power up by asserting the CS signal low and cannot be changed as long as the part is powered on. The SPI standard defines the physical link only. And not the complete data transfer protocol. The SPI implementation uses the same command set of the SD mode. The SPI mode consists of the following four signals:

— **CS:** Host to card Chip Select signal.
— **CLK:** Host to card clock signal
— **DataIn:** Host to card data signal.
— **DataOut:** Card to host data signal.

From the application point of view, the advantage of the SPI mode is the capability of using an off-the-shelf host that reducing the design-in effort to minimum. The disadvantage is the loss of performance, relatively to the SD- mode which enables the wide bus option

SD Memory Card system (SPI mode) bus topology

Another SPI common characteristic are byte transfers, which is implemented in the card as well. All data tokens are multiples of bytes (8 bit) aligned to the CS signal.

7. SD Card Pin Assignment

Pin #	Name	Type[1]	micro SD/SDHC Description
1	DAT2	I/O/PP	Data Line [Bit 2]
2	CD/DAT3	I/O/PP3	Card Detect / Data Line [Bit 3]
3	CMD	PP	Command / Response
4	VDD	S	Supply voltage
5	CLK	I	Clock
6	Vss	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line [Bit 0]
8	DAT1	I/O/PP	Data Line [Bit 1]

Pin Assignment in SD Bus Mode Pad Definition

Pin #	Name	Type	micro SD/SDHC Description
1	RSV	-	Reserved
2	CS	I	Chip Select
3	DI	S	Data In
4	VDD	S	Supply Voltage
5	SCLK	I	Clock
6	VSS	S	Supply Voltage Ground
7	DO	O	Data Out
8	RSV	I	Reserved

Pin Assignment in SPI Bus Mode Pad Definition

Note: 1. S: power supply; I: input; O: output; PP: I/O using push-pull drivers

2. The extended DAT lines (DAT1 -DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used. It is defined so, in order to keep compatibility to MultiMedia Cards.

3. At power up this line has a 50KOhm pull up enabled in the card. This resistor serves two functions Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user, during regular data transfer, with SEND_IF_COND (CMD8) SET_CLR_CARD_DETECT (ACMD42) command

4. DAT1 line may be used as Interrupt Output (from the Card) in SDIO mode during all the times that it is not in use for data transfer operations (refer to "SDIO Card Specification" for further details).

Registers

Name	Width	Description
CID	128	Card identification number: individual card number for identification
RCA	16	Relative card address: local system address of a card dynamically suggested by the card and approved by the host during initialization
CSD	128	Card specific data: information about the card operation conditions
SCR	64	SD Configuration Register: information about the SD Card's special feature capabilities
OCR	32	Operation Condition Register

SD Memory Card registers

Note: 1. RCA register is not used (available) in SPI mode.

8. Card Registers

Within the card interface six registers are defined：OCR, CID, CSD, RCA, DSR and SCR. These can be accessed only by corresponding commands. The OCR, CID, CSD and SCR registers carry the card/content specific information, while the RCA and DSR configuration registers storing actual configuration parameters.

OCR Register

The 32-bit operation conditions register stores the V_{DD} voltage profile of the card. In addition, this register includes a status information bit. This status bit is set if the card power up procedure has been finished. The OCR register shall be implemented by the cards which do not support the full operation voltage range of the SD Memory Card bus, or if the card power up extends the definition in the timing diagram.

OCR bit position	VDD voltage window
0-3	reserved
4	reserved
5	reserved
6	reserved
7	Reserved for Low Voltage Range
8	reserved
9	reserved
10	reserved
11	reserved
12	reserved
13	reserved
14	reserved
15	2.7-2.8
16	2.8-2.9
17	2.9-3.0
18	3.0-3.1
19	3.1-3.2
20	3.2-3.3
21	3.3-3.4
22	3.4-3.5
23	3.5-3.6
24-29	reserved
30	Card Capacity Status (CCS) 1
31	card power up status bit（busy）[2]

OCR register definition

- (1) This bit is valid only when the card power up status bit is set.

- (2) The supported voltage range is coded as shown in Table above: A voltage range is not supported if the corresponding bit value is set to Low. As long as the card is busy, the corresponding bit (31) is set to LOW.

CID Register

The Card Identification (CID) register is 128 bits wide. It contains the card identification information used during the card identification phase. Every individual flash card shall have a unique identification number. The structure of the CID register is defined in the following paragraphs

CID Bit	Width	Name	Field
[127:120]	8	Manufacture ID	MID
[119:104]	16	OEM/Application ID	OID
[103:64]	40	Product Name	PNM
[63:56]	8	Product Revision	PRV
[55:24]	32	Product Serial Number	PSN
[23:20]	4	Reserved	---
[19:8]	12	Manufacturing Date	MDT
[7:1]	7	CRC7 check sum	CRC
[0]	1	Not used, always'1'	---

The CID fields

MID

An 8 bit binary number that identifies the card manufacturer. The MID number is controlled, defined and allocated to a SD Memory Card manufacturer by the SD Group. This procedure is established to ensure uniqueness of the CID register.

OID

A 2 ASCII string characters that identifies the card OEM and/or the card contents (when used as a distribution media either on ROM or FLASH cards). The OID number is controlled, defined and allocated to a SD Memory Card manufacturer by the SD Group. This procedure is established to ensure uniqueness of the CID register.

PNM

The product name is a string, 5 ASCII characters long.

PRV

The product revision is composed of two Binary Coded Decimal (BCD) digits, four bits each, representing an "n.m" revision number. The "n" is the most significant nibble and "m" is the least significant nibble.

PSN

The Serial Number is 32 bits of unsigned binary integer.

MDT

The manufacturing date composed of two hexadecimal digits, one is 8 bit representing the year（y） and

the other is four bits representing the month（m）.

The "m" field 【11:8】is the month code .1 = January.

The "y" field【19:12】is the year code .0 = 2000.

CRC

CRC7 checksum value (7 bits. This is the checksum of the CID contents computed,).

CSD Register

The Card-Specific Data register provides information on how to access the card contents. The CSD defines the data format, error correction type, maximum data access time; data transfer speed, whether the DSR register can be used etc. The programmable part of the register (entries marked by W or E, see below) can be changed by CMD27. The types of the entries in the table below are coded as follow: R = readable, W (1) = writable once, W = multiple writable.

Name	Field	Width	Cell Type	CSD-slice
CSD structure	CSD_STRUCTURE	2	R	【127：126】
reserved	--	6	R	【125：120】
Data read access-time-1	TAAC	8	R	【119：112】
Data read access-time-2 in CLK cycles（NSAC*100）	NSAC	8	R	【111：104】
max. data transfer rate	TRAN_SPEED	8	R	【103：96】
card command classes	CCC	12	R	【95：84】
max. read data block length	READ_BL_LEN	4	R	【83：80】
partial blocks for read allowed	READ_BL_PARTIAL	1	R	【79：79】
write block misalignment	WRITE_BLK_MISALIGN	1	R	【78：78】
read block misalignment	READ_BLK_MISALIGN	1	R	【77：77】
DSR implemented	DSR_IMP	1	R	【76：76】
reserved	--	2	R	【75：74】
device size	C_SIZE	12	R	【73：62】
max .read current at V_{DD} min	VDD_R_CURR_MIN	3	R	【61：69】
max .read current at V_{DD} max	VDD_R_CURR_MAX	3	R	【58：56】
max. write current at V_{DD} min	VDD_W_CURR_MIN	3	R	【55：53】
device size multiplier	C_SIZE_MULT	3	R	【49：47】
erase single block enable	ERASE_BLK_EN	1	R	【46：46】
erase sector size	SECTOR_SIZE	7	R	【45：39】
write protect group size	WP_GRP_SIZE	7	R	【38：32】

write protect group enable	WP_GRP_ENABLE	1	R	【31：31】
Reserved for MultiMediaCard compatibility		2	R	【30：29】
write speed factor	R2W_FACTOR	3	R	【28：26】
max. write data block length	WRITE_BL_LEN	4	R	【25：22】
partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	【21：21】
reserved	--	5	R	【20：16】
File format group	FILE_FORMAT_GRP	1	R/W(1)	【15：15】
copy flag (OTP)	COPY	1	R/W(1)	【14：14】
permanent write protection	PERM_WRITE_PROTECT	1	R/W(1)	【13：13】
temporary write protection	TMP_WRITE_PROTECT	1	R/W	【12：12】
File format	FILE_FORMAT	2	R/W(1)	【11：10】
reserved		2	R/W	【9：8】
CRC	CRC	7	R/W	【7：1】
not used, always'1'	--	1	--	【0：0】

The CSD Register fields

The following sections describe the CSD fields and the relevant data types. If not explicitly defined otherwise, all bit strings are interpreted as binary coded numbers starting with the left bit first.

CSD_STRUCTURE

Version number of the related CSD structure.

CSD_STRUCTURE	CSD structure version	Valid for SD Memory Card Physical Specification Version
0	CSD version 1.0	Version 1.01-1.10 Version 2.00/Standard Capacity
1	CSD version 2.0	Version 2.00/High Capacity
2-3	reserved	

CSD register structure

TAAC

Defines the asynchronous part of the data access time.

TAAC bit position	code
2：0	time unit 0=1ns,1=10ns,2=100ns,3=1μs,4=10μs, 5=100μs,6=1ms,7=10ms
6：3	time value 0=reserved, 1=1.0,2=1.2,3=1.3,4=1.5, 5=2.0,6=2.5,7=3.0,8=3.5,9=4.0,A=4.5, B=5.0,C=5.5,D=6.0,E=7.0,F=8.0
7	reserved

TAAC access time definition

TRAN SPEED

The following table defines the maximum data transfer rate per one data line - TRAN_SPEED：

TRAN_SPEED bit	code
2：0	transfer rate unit 0=100kbit/s, 1=1Mbit/s, 2=10Mbit/s, 3=100Mbit/s, 4…7=reserved
6：3	time value 0=reserved, 1=1.0,2=1.2,3=1.3,4=1.5, 5=2.0,6=2.5,7=3.0,8=3.5,9=4.0,A=4.5, B=5.0,C=5.5,D=6.0,E=7.0,F=8.0
7	reserved

Maximum data transfer rate definition

NSAC

Defines the worst case for the clock dependent factor of the data access time. The unit for NSAC is 100 clock cycles. Therefore, the maximal value for the clock dependent part of the data access time is 25.5k clock cycles. The total access time NAC as expressed in the Table 34 is the sum of TAAC and NSAC. It has to be computed by the host for the actual clock rate. The read access time should be interpreted as a typical delay for the first data bit of a data block or stream.

CCC

The SD Memory Card command set is divided into subsets (command classes). The card command class register CCC defines which command classes are supported by this card. A value of "1" in a CCC bit means that the corresponding command class is supported.

CCC bit	Supported card command class
0	class 0
1	class 1
……	
11	class 11

Supported card command classes

READ_BL_LEN

The maximum read data block length is computed as $2^{READ\_BL\_LEN}$. The maximum block length might therefore be in the range 512….2048 bytes. Note that in SD Memory Card the WRITE_BL_LEN is always equal to READ_BL_LEN.

READ_BL_LEN	Block length	Remark
0-8	reserved	
9	2^9 = 512 Bytes	
……	2^{11} = 2048 Bytes	
12-15	reserved	

Data block length

READ_BL_PARTIAL（always = 1 in SD Memory Card）

Partial Block Read is always allowed in SD Memory Card .It means that smaller block can be used as well. The Minimum block size will be one byte.

WRITE_BLK_MISALIGN

Defines if the data block to be written by command can be spread over more than one physical block of the memory device. The size of the memory block is defined in WRITE_BL_LEN.

WRITE_BLK_MISALIGN = 0 signals that crossing physical block boundaries is invalid.

WRITE_BLK_ MISALIGN = 1 signals that crossing physical block boundaries is allowed.

READ_BLK_MISALIGN

Defines if the data block to be read by one command can be spread over more than one physical block of the memory device. The size of the memory block is defined in READ_BL_LEN.

READ _BLK_MISALIGN = 0 signals that crossing physical block boundaries is invalid.

READ _BLK_ MISALIGN = 1 signals that crossing physical block boundaries is allowed.

DSR_IMP

Defined if the configurable driver stage is integrated on the card. If set a driver stage register（DSR）must be implemented also

DSR_IMP	DSR type
0	on DSR implemented
1	DSR implemented

DSR implementation code table

C_SIZE

This parameter is used to compute the user's data card capacity (not include the security protected area). The memory capacity of the card is computed from the entries C_SIZE , C_SIZE_MULT and READ_BL_LEN as follows：

memory capacity = BLOCKNR*BLOCK_LEN

where

BLOCKNR = （C_SIZE+1）*MULT

$MULT = 2^{C\_SIZE\_MULT+2}$ （C_SIZE_MULT < 8）

$BLOCK\_LEN = 2^{READ\_BL\_LEN}$ （READ_BL_LEN < 12）

Therefore the maximal capacity which can be coded is 4096*512*2048 = 4 GBs. Example: A 32 MByte card with BLOCK_LEN = 512 can be coded by C_SIZE_MULT = 3 and C_SIZE = 2000.

VDD_R_CURR_MIN , VDD_W_CURR_MIN

The maximum values for read and write currents at the minimal power supply V_{DD} are coded as follows：

VDD_R_CURR_MIN VDD_W_CURR_MIN	code for current consumption @ V_{DD}
2：0	0=0.5mA,1=1 mA,2=5 mA,3=10 mA,4=25 mA 5=35 Ma,6=60 mA,7=100 mA

$V_{DD, min}$ **current consumption**

VDD_R_CURR_MAX, VDD_W_CURR_MAX

The maximum values for read and write currents at the minimal power supply V_{DD} are coded as follows：

VDD_R_CURR_MAX VDD_W_CURR_MAX	code for current consumption @ V_{DD}
2：0	0=1mA,1=5mA,2=10mA,3=25mA,4=35 mA 5=45mA,6=80 mA,7=200 mA

$V_{DD, max}$ **current consumption**

C_SIZE_MULT

This parameter is used for coding a factor MULT for computing the total device size (see C_SIZE). The factor MULT is defined as $2^{C\_SIZE\_MULT+2}$.

C_SIZE_MULT	MULT	Remark
0	$2^2=4$	
1	$2^3=8$	
2	$2^4=16$	
3	$2^5=32$	
4	$2^6=64$	
5	$2^7=128$	
6	$2^8=256$	
7	$2^9=512$	

Multiply factor for the device size

ERASE_BLK_EN

Defines whether erase of one write block (see WRITE_BL_LEN) is allowed (beside the SECTOR_SIZE given below)

If ERASE_BLK_EN = 0 host can erase unit of SECTOR_SIZE.

If ERASE_BLK_EN = 1 host can erase unit of SECTOR_SIZE or unit of WRITE_BL_LEN.

SECTOR_SIZE

The size of erasable sector. The content of this register is a 7 bit binary coded value, defining the number of write block (see WRITE_BL_LEN). The actual size is computed by increasing this number by one. A value of zero means one write block, 127 means 128 write blocks.

WP_GRP_SIZE

The size of a write protected group. The content of this register is a 7 bit binary coded value, defining the number of erase sectors. The actual size is computed by increasing this number by one. A value of zero means 1 erase sector, 127 means 128 erase sectors.

WP_GRP_ENABLE

A value of "0" means no group write protection possible.

R2W_FACTOR

Defines the typical block program time as a multiple of the read access time. The following table defines the field format.

R2W_RACTOR	Multiples of read access time
0	1
1	2（write half as fast as read）
2	4
3	8
4	16
5	32
6,7	reserved

R2W_FACTOR

WRITE_BL_LEN

The maximum write data block length is computed as $2^{WRITE\_BL\_LEN.}$ The maximum block length might therefore be in the range from 512 up to 2048 bytes. Write Block Length of 512 bytes is always supported .

Note that in SD Memory Card the WRITE_BL_LEN is always equal to READ_BL_LEN.

WRITE_BL_LEN	Block length
0-8	Reserved
9	2^9=512 Bytes
10	2^{10}=1024 Bytes
11	2^{11}=2048 Bytes
12-15	reserved

Data block length

WRITE_BL_PARTIAL

Defines whether partial block sizes can be used in block write commands.

WRITE_BL_PARTIAL='0' means that only the WRITE_BL_LEN block size and its partial derivatives, in resolution of units of 512 bytes, can be used for block oriented data write.

WRITE_BL_PARTIAL='1' means that smaller blocks can be used as well. The minimum block size is one byte.

FILE_FORMAT_GRP

Indicates the selected group of file formats. This field is read-only for ROM. The usage of this field is shown in (see FILE_FORMAT).

COPY

Defines if the contents is original (='0') or has been copied (='1'). The COPY bit for OTP and MTP devices, sold to end consumers, is set to '1' which identifies the card contents as a copy. The COPY bit is an one time programmable bit.

PERM_WRITE_PROTECT

Permanently protects the whole card content against overwriting or erasing (all write and erase commands for card is permanently disabled). The default value is '0', i.e. not permanently write protected.

TMP_WRITE_PROTECT

Temporarily protects the whole card content from being overwritten or erased (all write and erase commands for this card are temporarily disabled). This bit can be set and reset. The default value is '0', i.e. not write protected.

FILE_FORMAT

Indicates the file format on the card. This field is read-only for ROM. The following formats are defined：

FILE_FORMAT_GRP	FILE_FORMAT	Type
0	0	Hard disk-like file system with partition table
0	1	DOS FAT (floppy-like) with boot sector only (no partition table)
0	2	Universal File Format
0	3	Others / Unknown
1	0,1,2,3	Reserved

File formats

CRC

The CRC field carries the check sum the CSD contents.

The checksum has to be recalculated by the host for any CSD modification. The default corresponds to the initial CSD contents.

The following table lists the correspondence between the CSD entries and the command classes. A '+' entry indicates that the CAD field affects the commands of the related command class.

CSD Field	Command classes							
	0	2	4	5	6	7	8	9
CSD_STRUCTURE	+	+	+	+	+	+	+	+
TAAC		+	+	+	+	+	+	
NSAC		+	+	+	+	+	+	
TRAN_SPEED		+	+					
CCC	+	+	+	+	+	+	+	+
READ_BL_LEN		+						
WRITE_BLK_MISALIGN			+					
READ_BLK_MISALIGN		+						
DSR_IMP	+	+	+	+	+	+	+	+
C_SIZE_MANT		+	+	+	+	+	+	
C_SIZE_EXP		+	+	+	+	+	+	
VDD_R_CURR_MIN		+						
VDD_R_CURR_MAX		+						
CSD Field	Command classes							
	0	2	4	5	6	7	8	9
VDD_W_CURR_MIN			+	+	+	+	+	
VDD_W_CURR_MAX			+	+	+	+	+	
ERASE_BLK_EN				+	+	+	+	
SECTOR_SIZE				+	+	+	+	
WP_GRP_SIZE					+	+	+	
WP_GRP_ENABLE					+	+	+	
R2W_FACTOR			+	+	+	+	+	
WRITE_BL_LEN			+	+	+	+	+	
WRITE_BL_PARTIAL			+	+	+	+	+	
FILE_FORMAT_GRP								
COPY	+	+	+	+	+	+	+	+

PERM_WRITE_PROTECT	+	+	+	+	+	+	+	+
TMP_WRITE_PROTECT	+	+	+	+	+	+	+	+
FILE_FORMAT								
CRC	+	+	+	+	+	+	+	+

Cross reference of CSD fields vs. command classes

RCA Register

The writable 16-bit relative card address register carries the card address that is published by the card during the card identification. This address is used for the addressed host-card communication after the card identification procedure. The default value of the RCA register is 0x0000.The value 0x0000 is reserved to set all cards into the *Stand-by State* with CMD7.

DSR Register (Optional)

DSR register is a 16-bit driver stage register. It can be optionally used to improve the bus performance for extended operating conditions (depending on parameters like bus length, transfer rate or number of card). The CSD register carries the information about the DSR register usage. The default value of the DSR register is 0x404.

SCR Register

In addition to the CSD register there is another configuration register that named - SD CARD Configuration Register (SCR). SCR provides information on SD Memory Card's special features that were configured into the given card. The size of SCR register is 64 bit. This register shall be set in the factory by the SD Memory Card manufacturer.

The following table describes the SCR register content.

Description	Field	Width	Cell Type	SCR Slice
SCR Structure	SCR_STRUCTURE	4	R	【63：60】
SD Memory Card–Spec. Version	SD_SPEC	4	R	【59：56】
Data status after erases	DATA_STAT_AFTER_ERASE	1	R	【55：55】
SD Security Support	SD_SECURITY	3	R	【54：52】
DAT Bus width supported	SD_BUS_WIDTHS	4	R	【51：48】
reserved	--	16	R	【47：32】
Reserved for manufacturer usage	--	32	R	【31：0】

The SCR Fields

SCR_STRUCTURE

Version number of the related SCR structure in the SD Memory Card Physical Layer Specification.

CSD_STRUCTURE	CSD structure version	Valid for SD Physical Layer Specification Version
0	SCR version No.1.0	Version 1.0
1-15	reserved	

SCR register structure version

SD_SPEC

Describes the SD Memory Card Physical Layer Specification version supported by this card.

SPEC_VERS	Physical Layer Specification Version Number
0	Version 1.0-1.01
1	Version 1.10
2	Version 2.00
3-15	reserved

SD Memory Card Physical Layer Specification Version

DATA_STAT_AFTER_ERASE

Defines the data status after erase, whether it is '0' or '1' (the status is card vendor dependent).

SD_SECURITY

Describes the security algorithm supported by the card.

SD_SECURITY	Supported algorithm
0	No security
1	Not Used
2	Version 1.01
3	Version 2.00
4..7	reserved

SD Supported security algorithm

SD_BUS_WIDTHS

Describes all the DAT bus widths that are supported by this card.

SD_BUS_WIDTHS	Supported Bus Widths
Bit 0	1 bit（DAT0）
Bit 1	reserved
Bit 2	4 bit（DAT0-3）
Bit 3【MSB】	reserved

SD Memory Card Supported Bus Widths

Since SD Memory Card shall support at least the two bus modes 1bit or 4bit width then any SD Card shall set at least bits 0 and 2.

9. SD Card Dimension
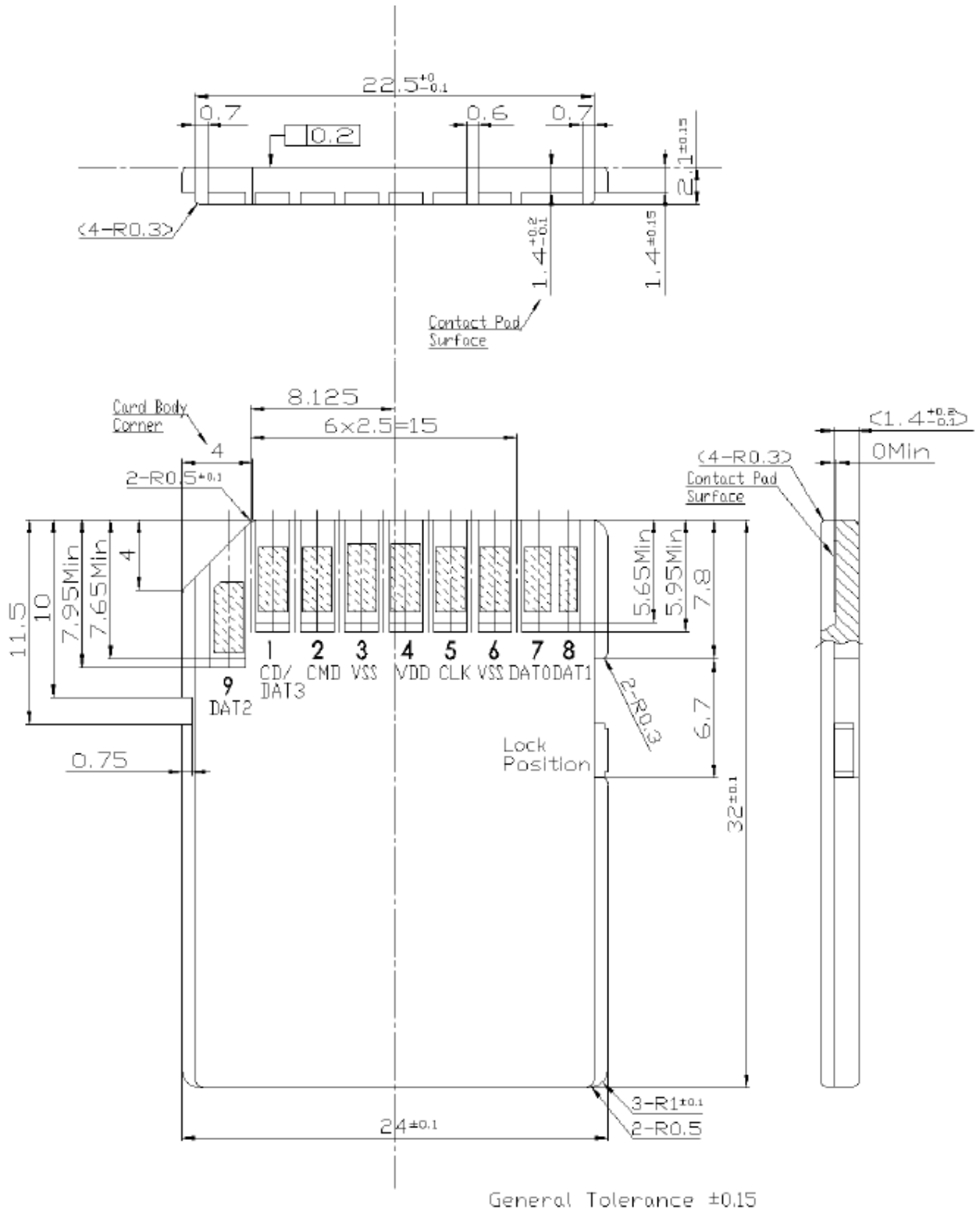
SD Memory Card - Mechanical Description

Type	Measurement
Length	32.00mm +/- 0.10mm
Width	24.00mm +/- 0.10mm
Thickness	2.10mm +/- 0.15mm

SD card physical dimension (Unit in mm)